Current-mode Driving Schemes for AMOLED Display & SIMO PMICs

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October 10th, 2012

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- Feedback Driving Method
  - -DFFC Driver
- Feedforward Driving Methods
  - -TCF Driver
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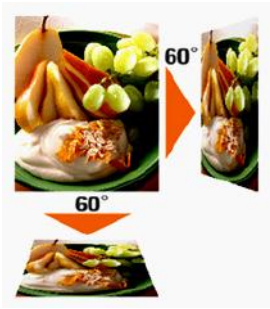
- Real-time Image Sticking Compensation Methods
- PMIC

Motivation (1/2)

High Contrast



Natural Color

Wide Viewing Angle

AMOLED

(Active Matrix Organic Light Emitting Diode)

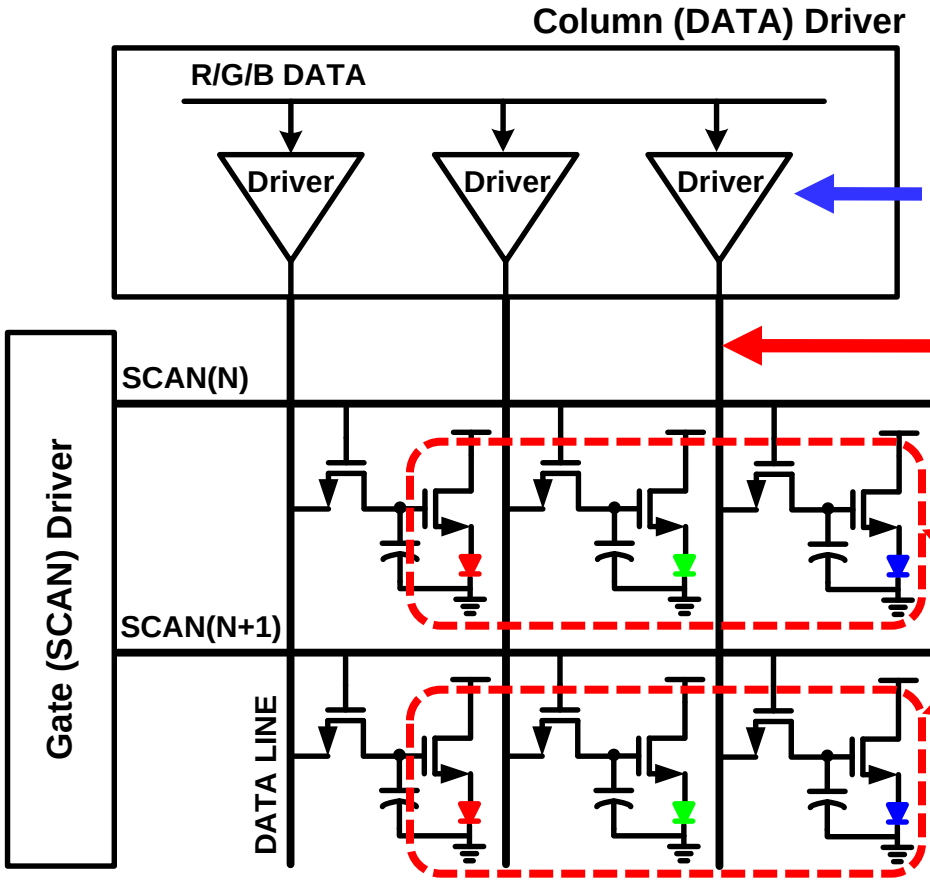
Fast Response

Thin

Low Power Consumption

Motivation (2/2)

AMOLED System

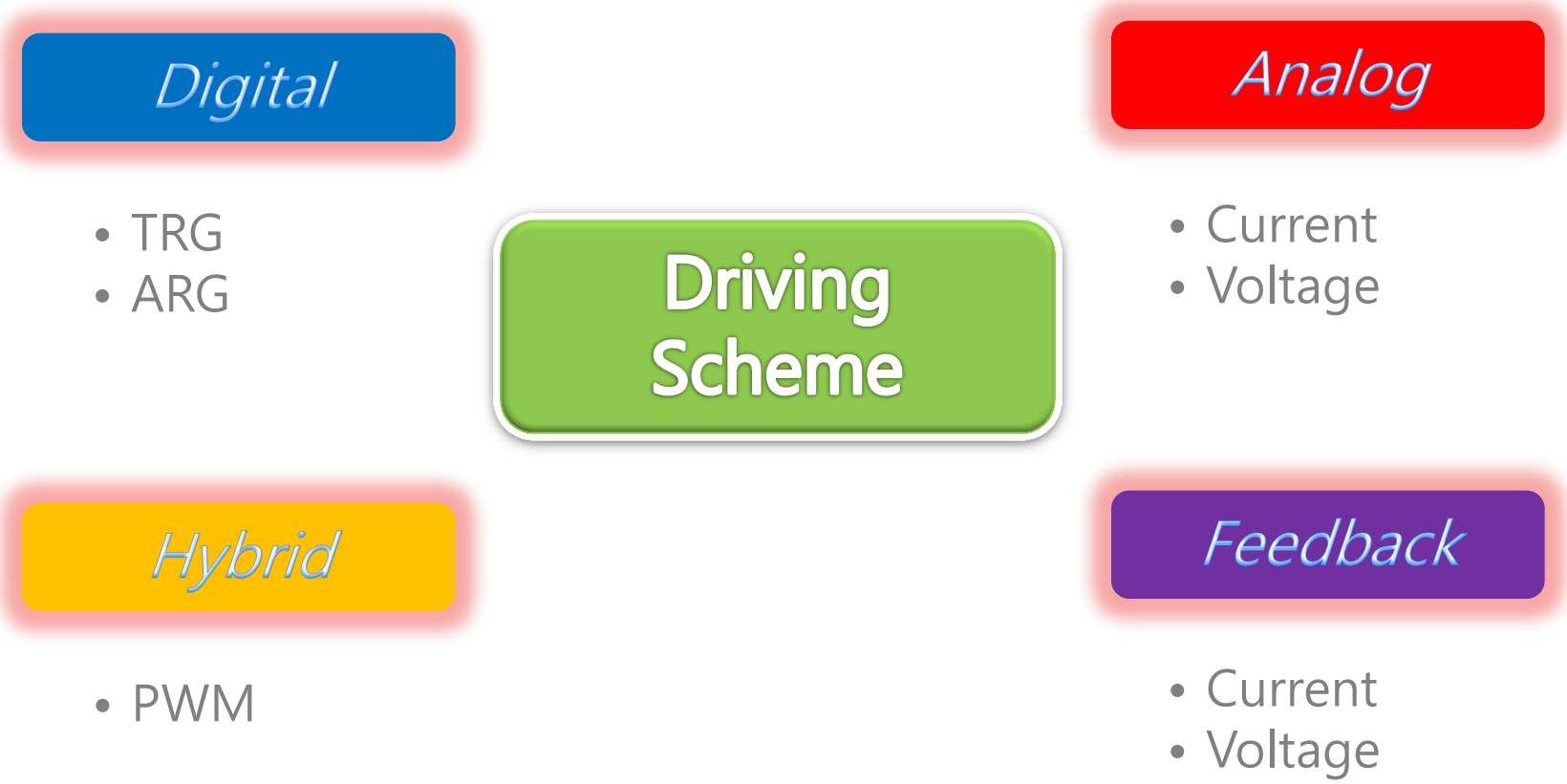


Requirements for Driver

1. Massive capacitance in data lines
2. Non-uniform TFT & Luminance

Introduction (1/2)

■ Data driving schemes for AMOLED displays



Introduction (2/2)

■ Data driving schemes for AMOLED displays

Conventional Driving Scheme							
	Analog Voltage	Analog Current	Digital ARG	Digital TRG	Voltage Feedback	Current Feedback	Hybrid PWM
Threshold Voltage Compensation	Good	Good	-	-	Good	Good	-
Mobility Compensation	Poor	Good	-	-	Good	Good	-
Driving Speed	Fast	Slow	Fast	Fast	Slow	Medium	Fast
Driving Accuracy	Medium	Good	Poor	Medium	Medium	Medium	Medium
Luminance Uniformity	Bad	Good	Good	Medium	Medium	Good	Medium

⇨ **High Speed Analog Current Driving Method**
High Driving Accuracy & Speed Current Feedback Method

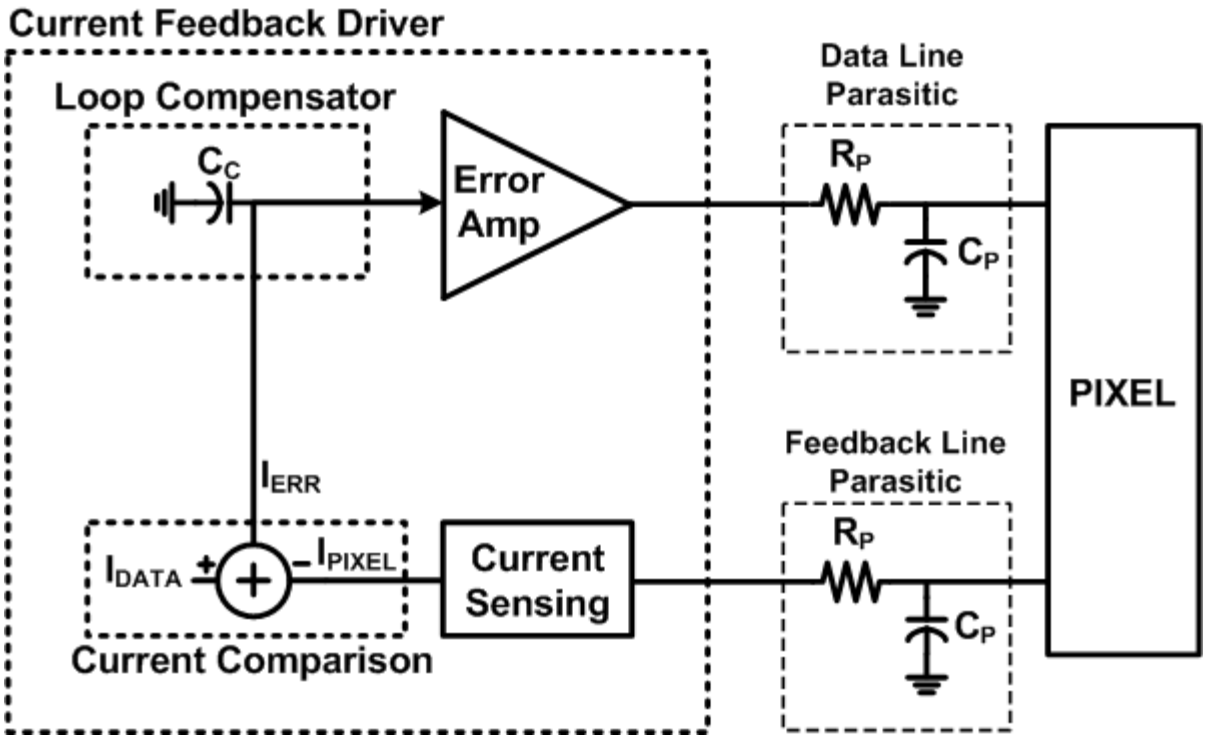
Part I

Current-mode AMOLED Drivers:
DFFC (Direct-type Fast Feedback Current) Driver

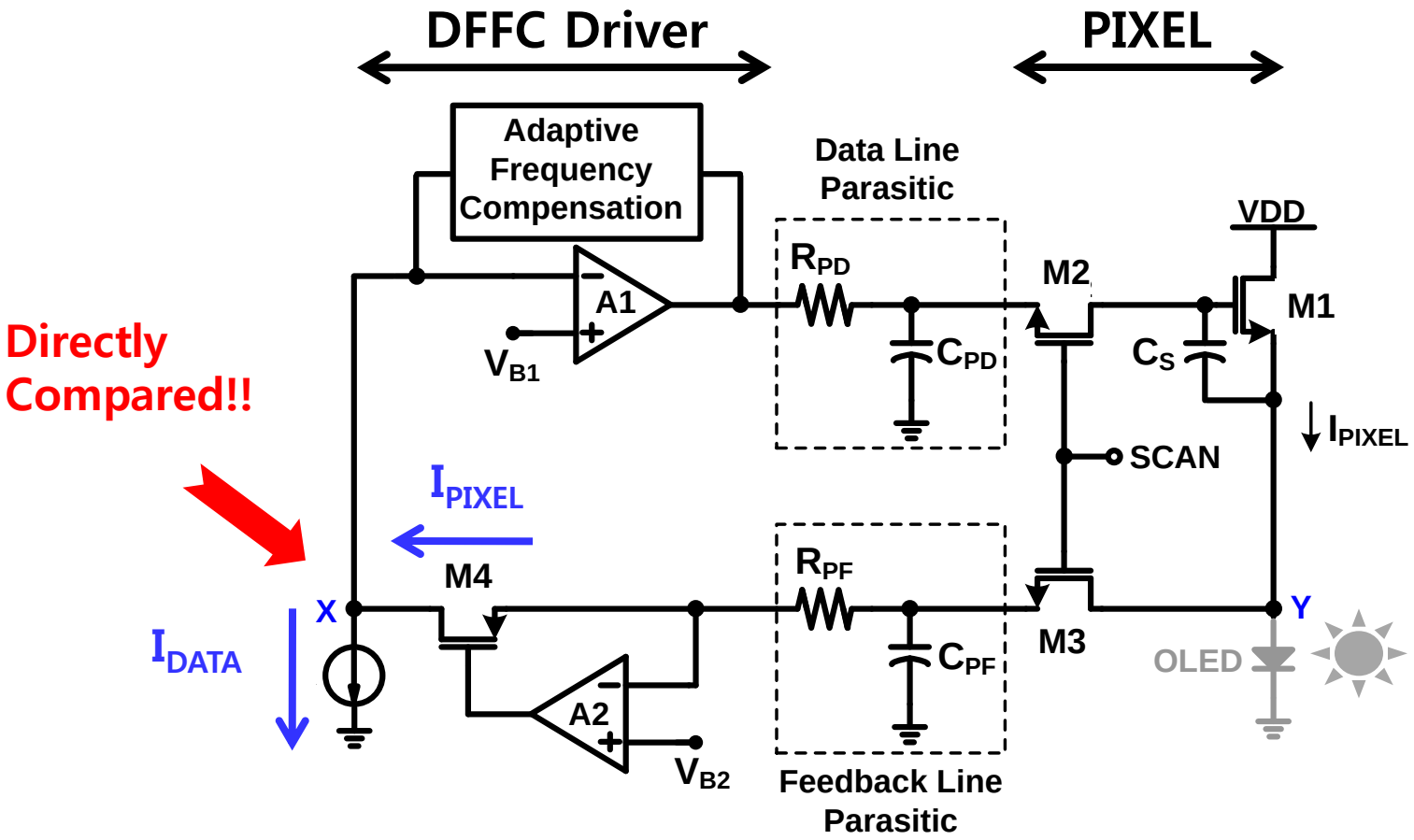
Block Diagram for FFCD

■ Conceptual diagrams for Fast Feedback Current Driver(FFCD)

Feedback driver : Current sensing & comparison,
loop compensator and error amp.

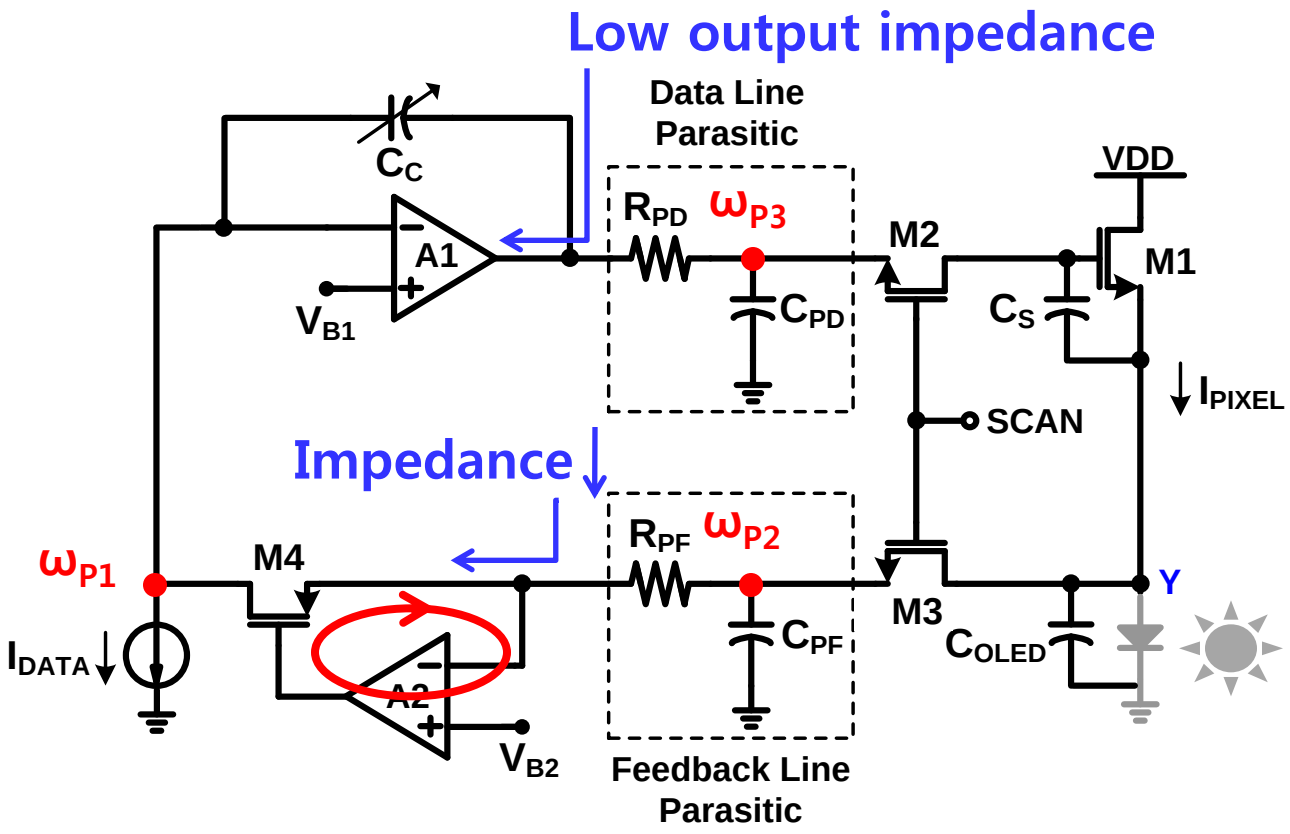


Direct-type Fast Feedback Current (DFFC) Driver



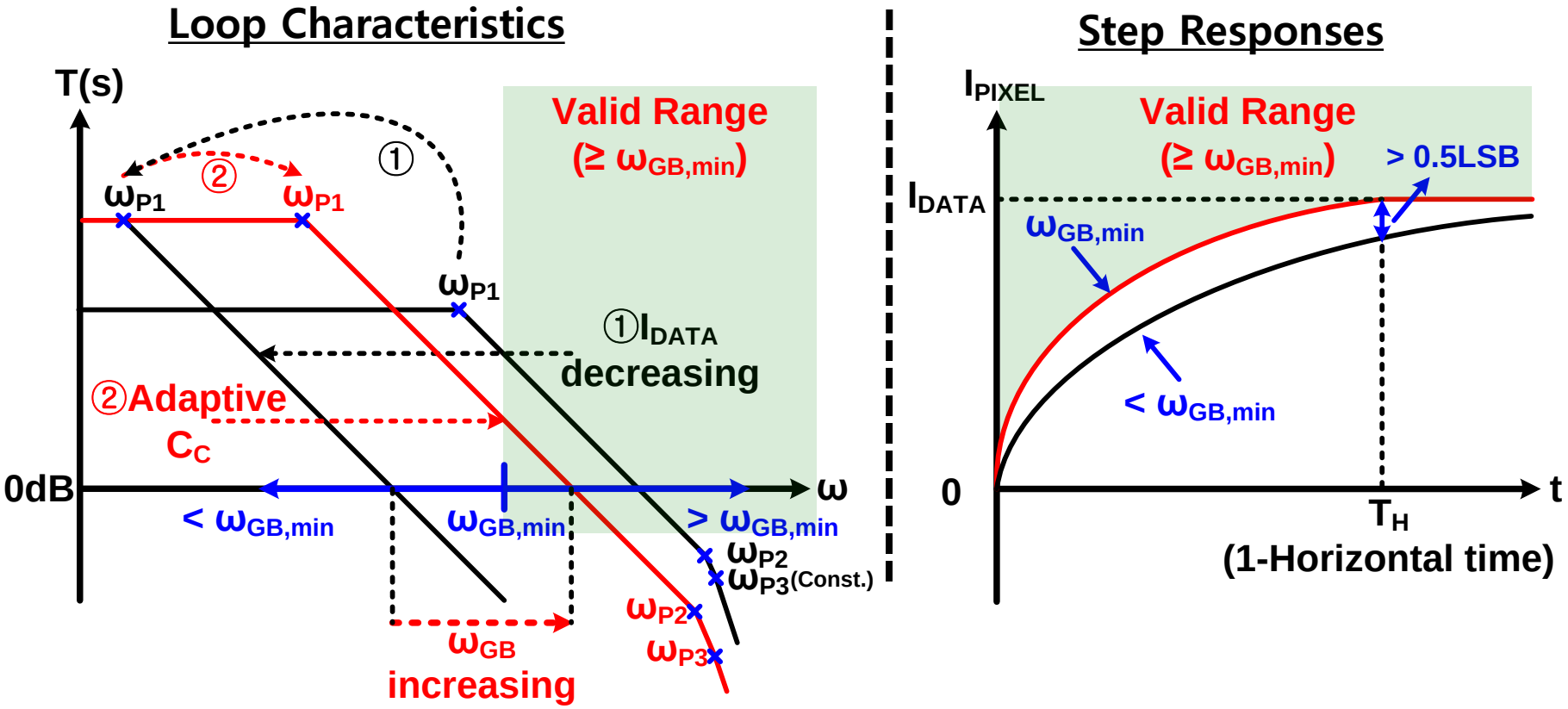
- $V_{B2} < V_{th,OLED}$
- OLED turns off during feedback loop operation

Delay Reduction from Capacitance



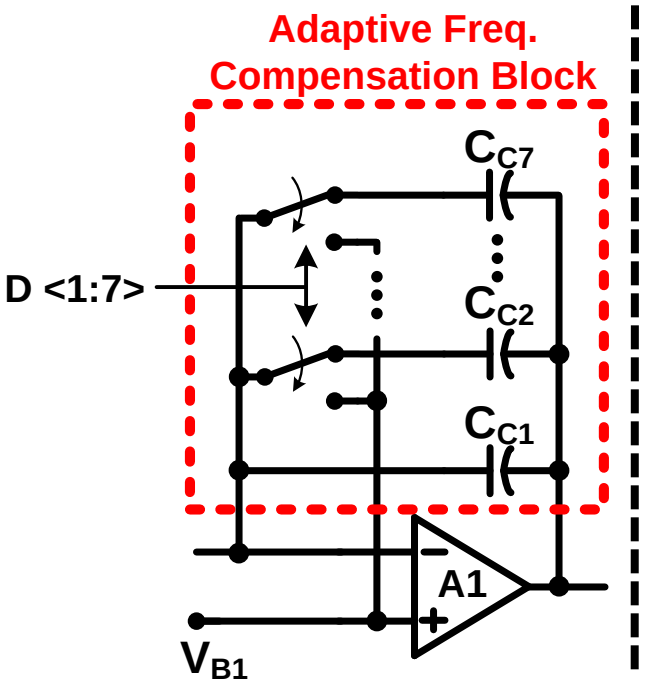
- Move 2nd,3rd poles to higher freq.
- Wider BW, faster driving speed

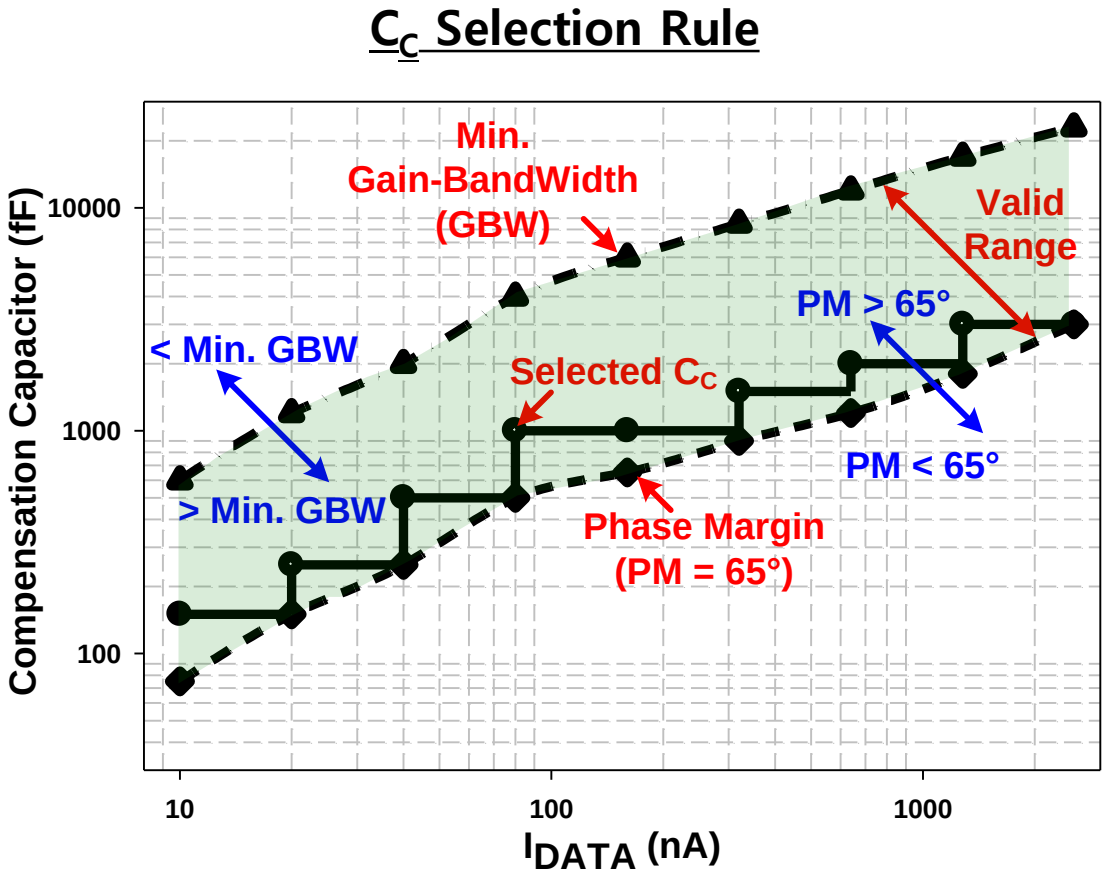
Requirement for Min. GBW



Display Resolution	Driving Accuracy	1-Horizontal time (T_H)	Min. Gain-BandWidth ($\omega_{GB,min}$)
WXGA (1280 X 800)	8b	20μs @60Hz	50kHz
FHD (1920 X 1080)	8b	15μs @60Hz	66kHz

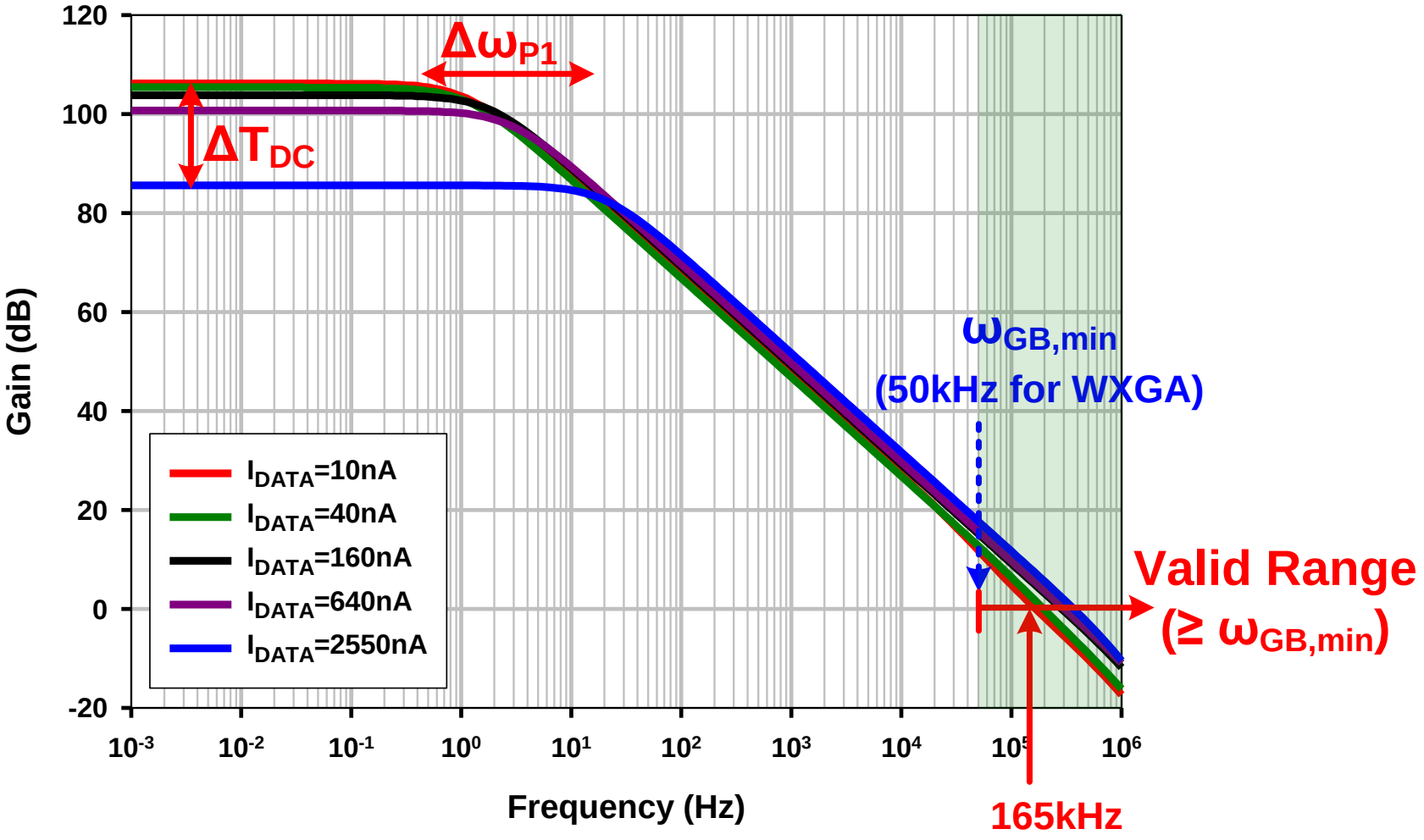
Adaptive Freq. Compensation



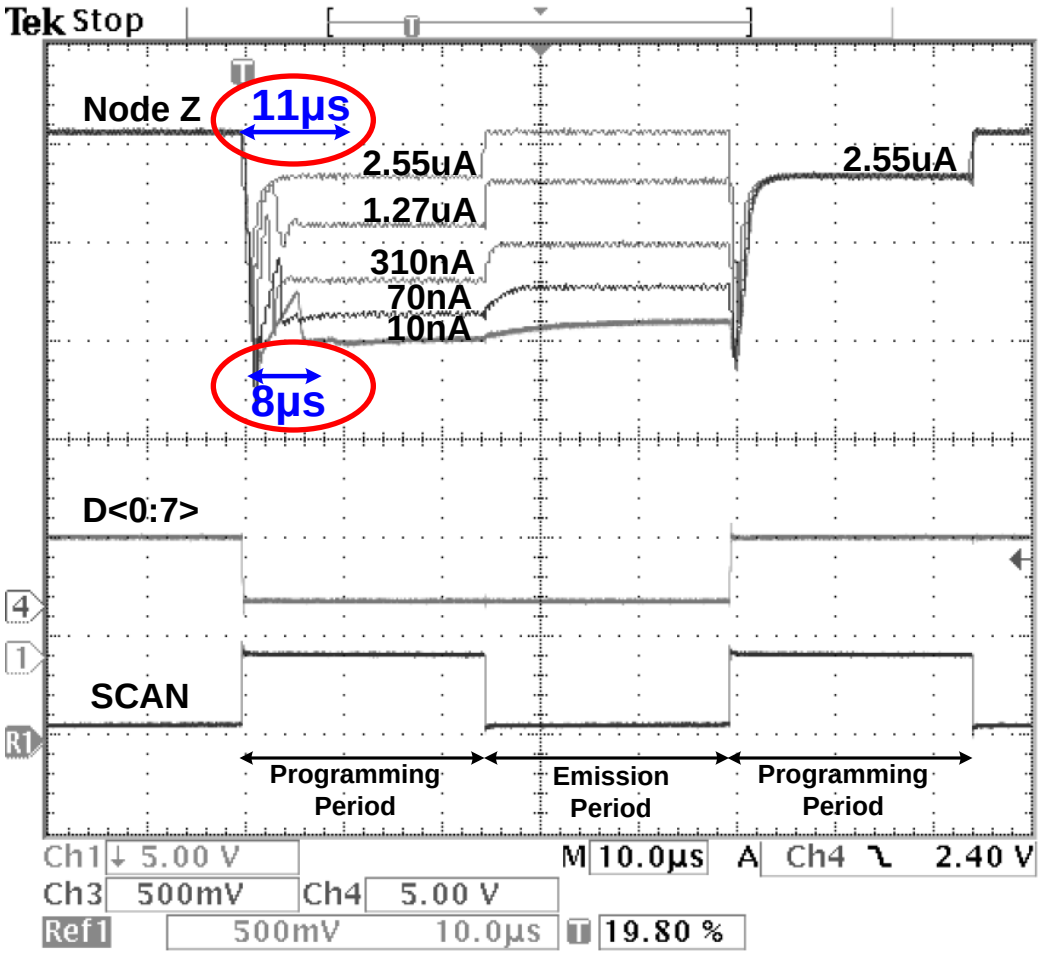


- Compensation capacitor (C_C) array
- Cc from GBW and PM boundary conditions
- Divide 7 ranges according to I_{DATA}

Loop Gain with Full I_{DATA} Range



Measurement Result (Data Transition)

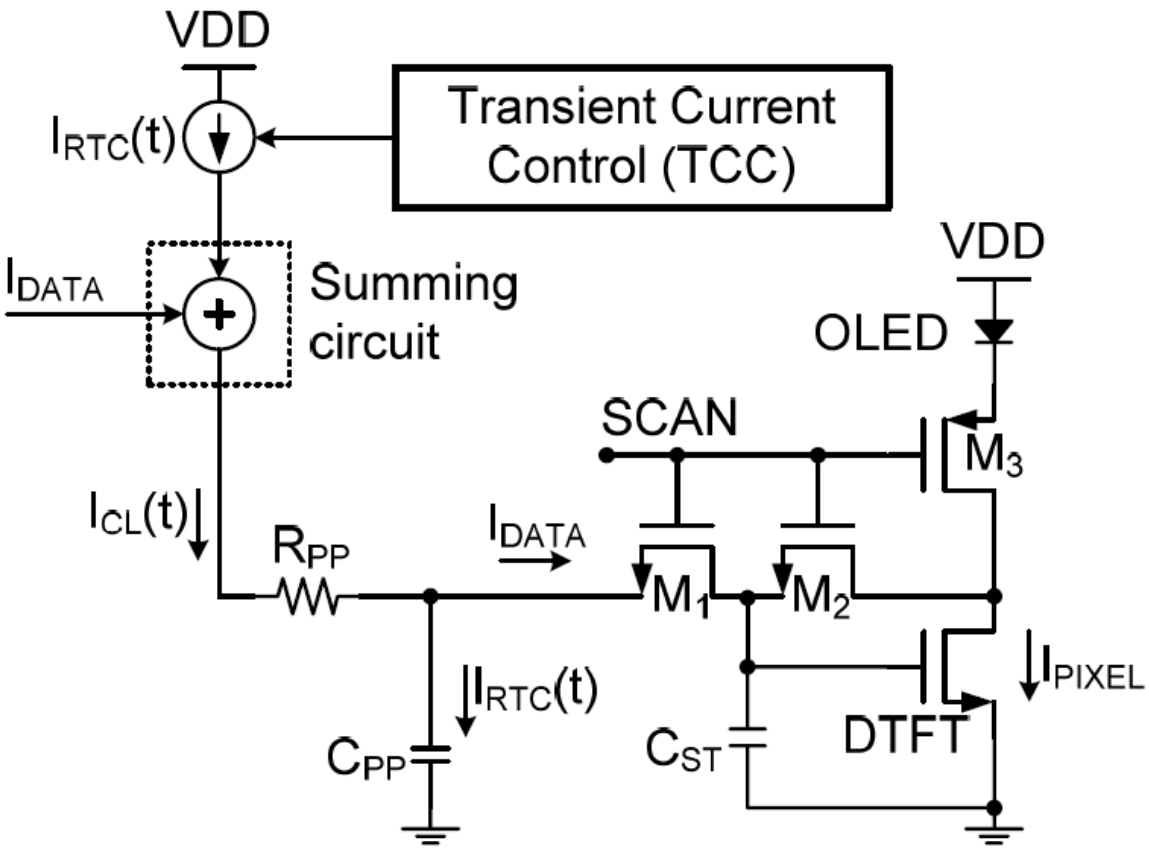


- Data current range from 10nA to 2.55µA
- Settling time < 11µs

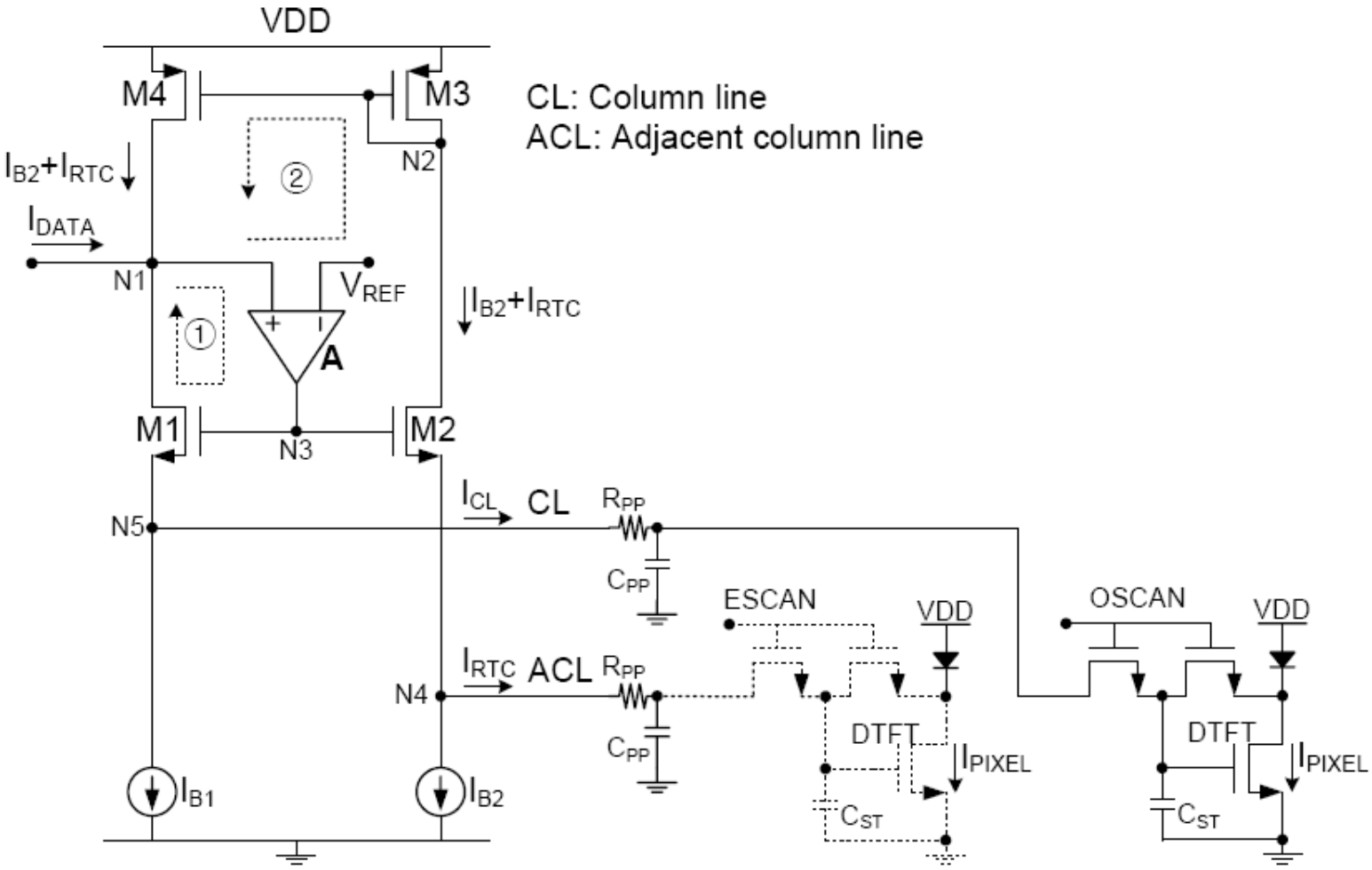
Part II

Current-mode AMOLED Drivers:
TCF (Transient Current Feedforward) Driver

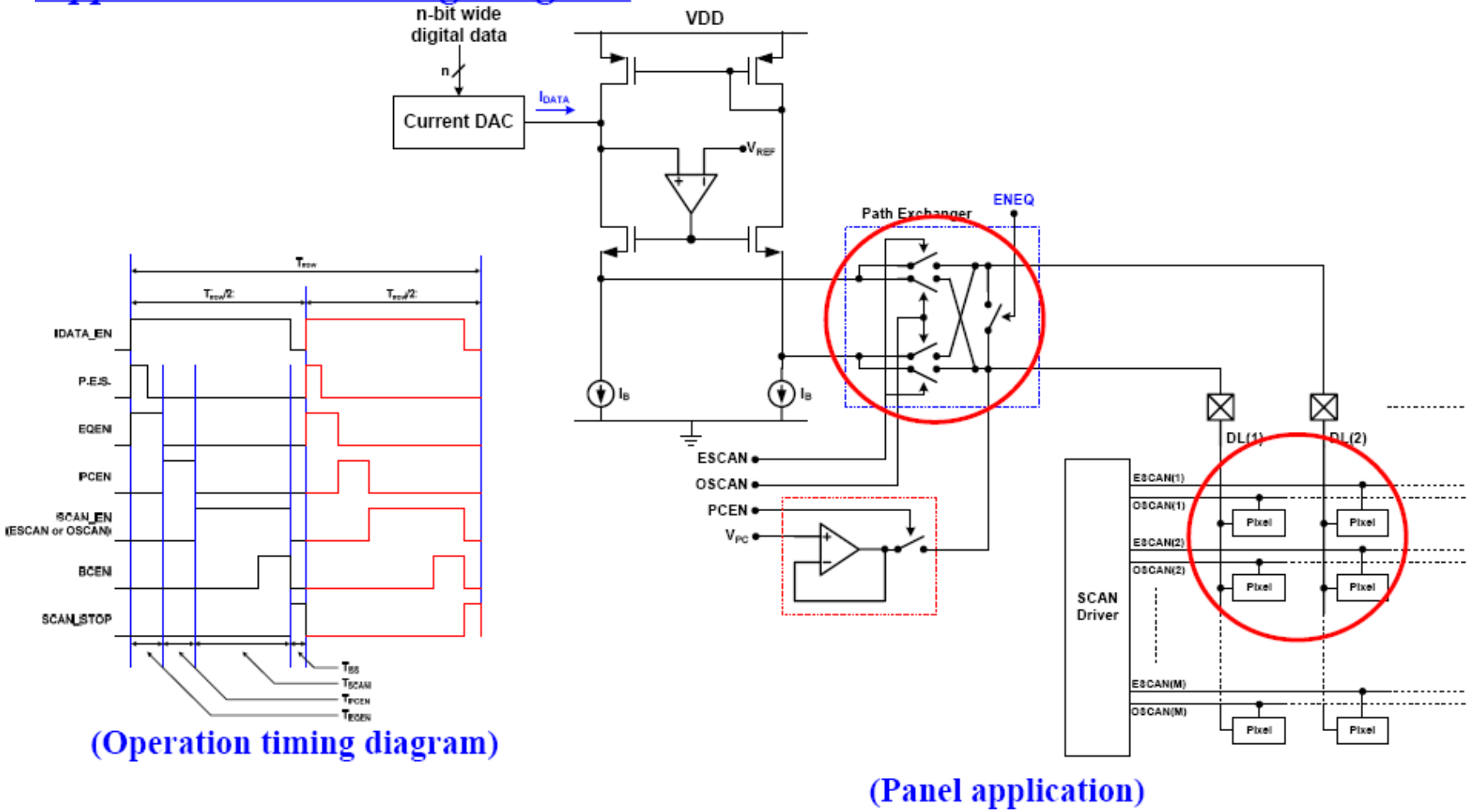
Introduction of the TCC



Realization of the TCC



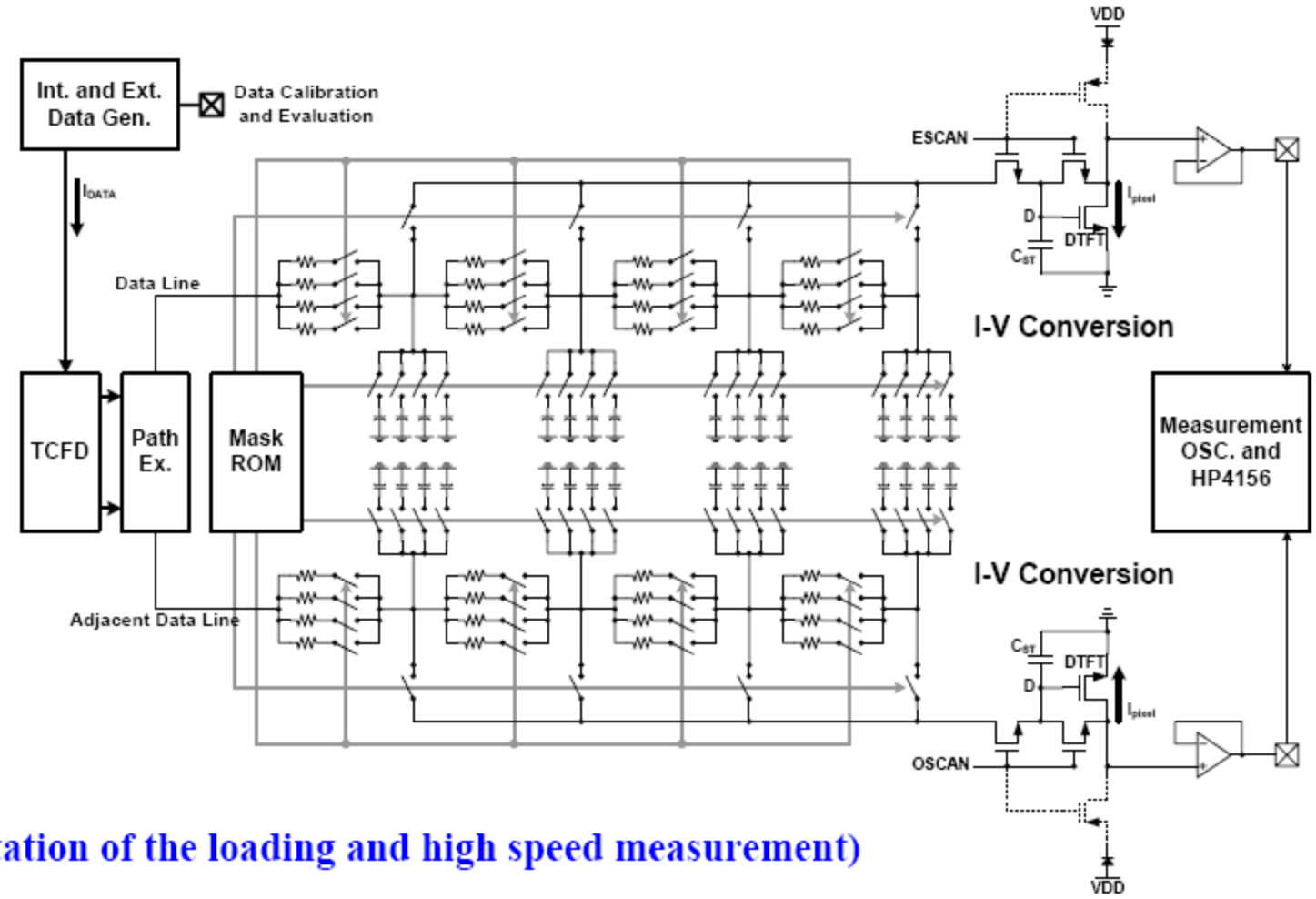
Application and Timing Diagram



(Operation timing diagram)

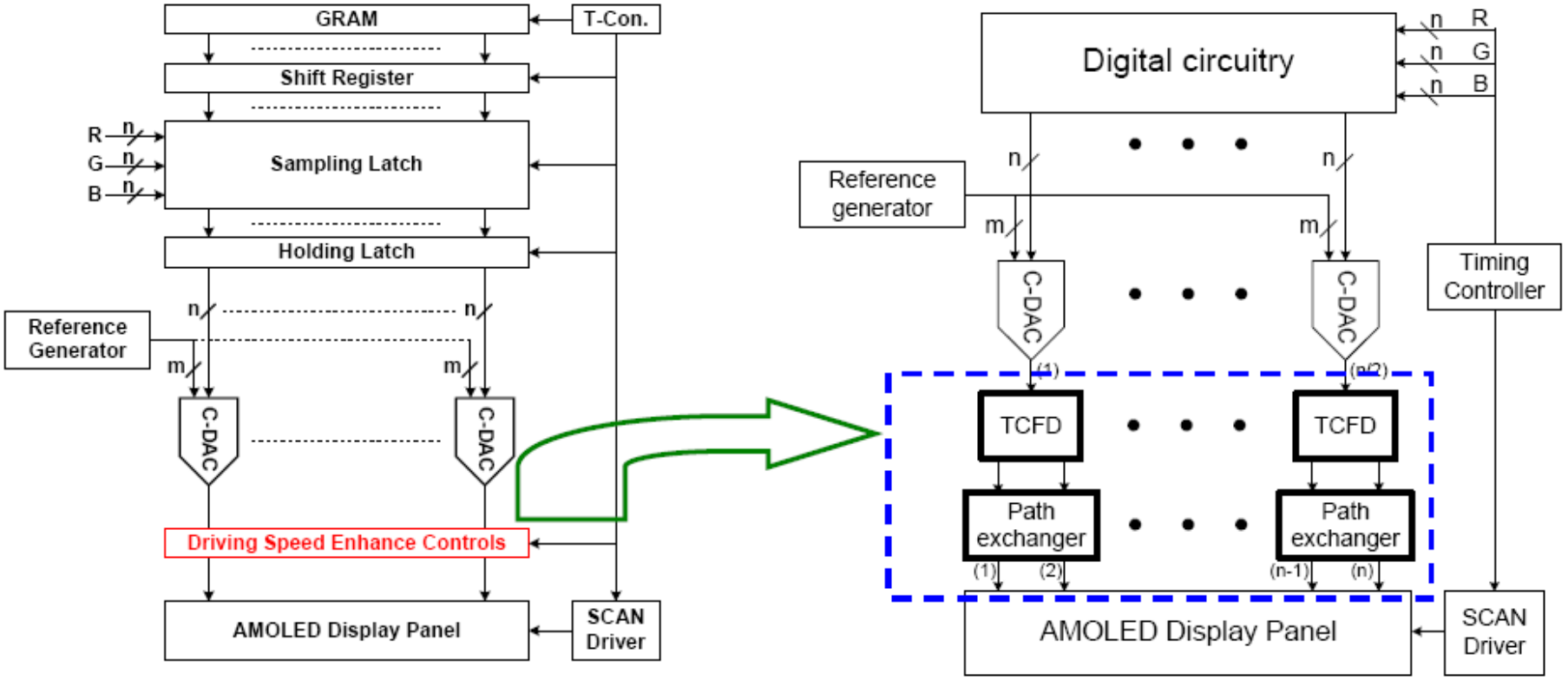
(Panel application)

Display Panel Emulation:

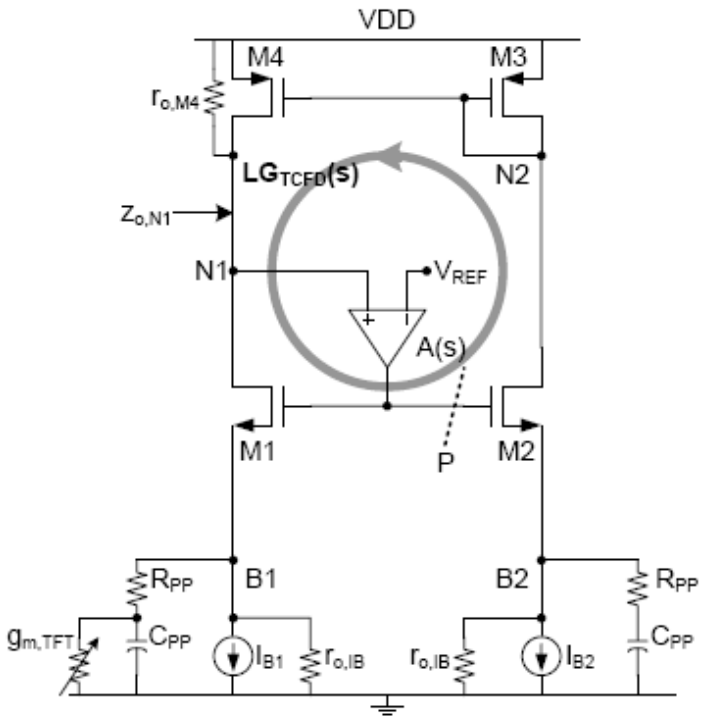


(Implementation of the loading and high speed measurement)

Driver Architecture with TCFD and Path Exchanger



Stability



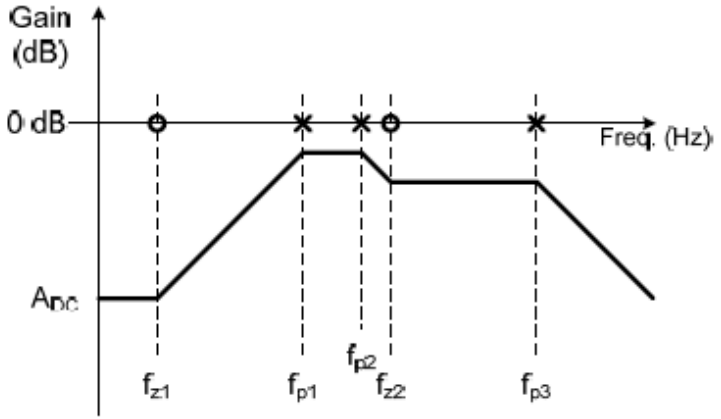
$$z_{o,N1} \approx \frac{1}{A(s)} \cdot \frac{1}{g_{m,TFT}} \cdot \frac{\left(1+s\frac{C_{PP}}{g_{m,M1}}\right)}{\left(1+s\frac{C_{PP}}{g_{m,TFT}}\right)}$$

$$LG_{TCFD} = \frac{z_{o,N1}}{\frac{1}{g_{m,M2}} + r_{o,IB} \,//\, \frac{1}{sC_{PP}}} \cdot A(s)$$

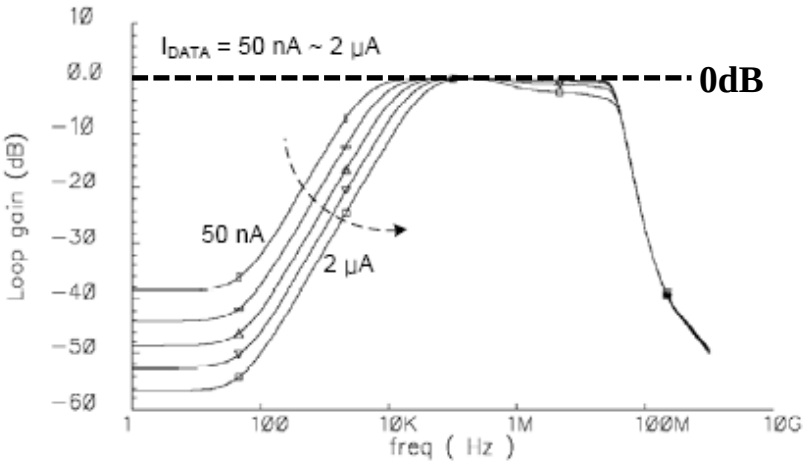
$$\approx \frac{1}{g_{m,TFT} r_{o,IB}} \cdot \frac{\left(1+sC_{PP}r_{o,IB}\right) \cdot \left(1+s\frac{C_{PP}}{g_{m,M1}}\right)}{\left(1+s\frac{C_{PP}}{g_{m,TFT}}\right) \cdot \left(1+s\frac{C_{PP}}{g_{m,M2}}\right)}$$

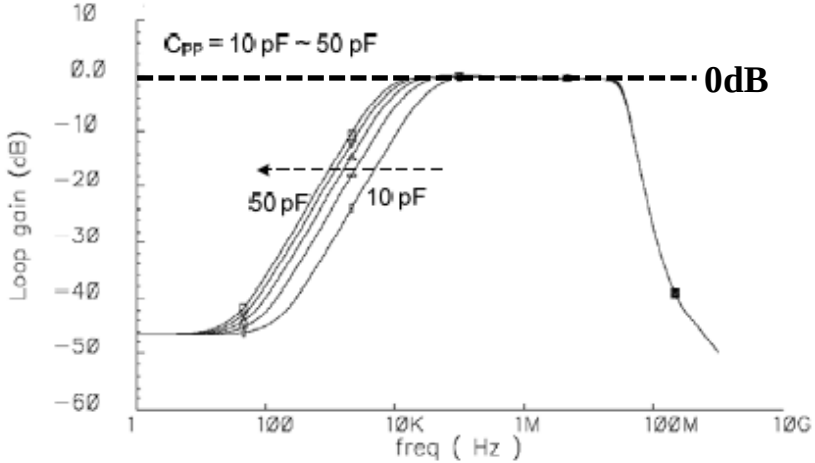
The loop gain is always below 0 dB

Verification by Simulation



$$LG_{TCFD} \approx \frac{1}{g_{m,TFT} r_{o,IB}} \cdot \frac{\left(1+sC_{PP}r_{o,IB}\right)\cdot\left(1+s\frac{C_{PP}}{g_{m,M1}}\right)}{\left(1+s\frac{C_{PP}}{g_{m,TFT}}\right)\cdot\left(1+s\frac{C_{PP}}{g_{m,M2}}\right)}$$



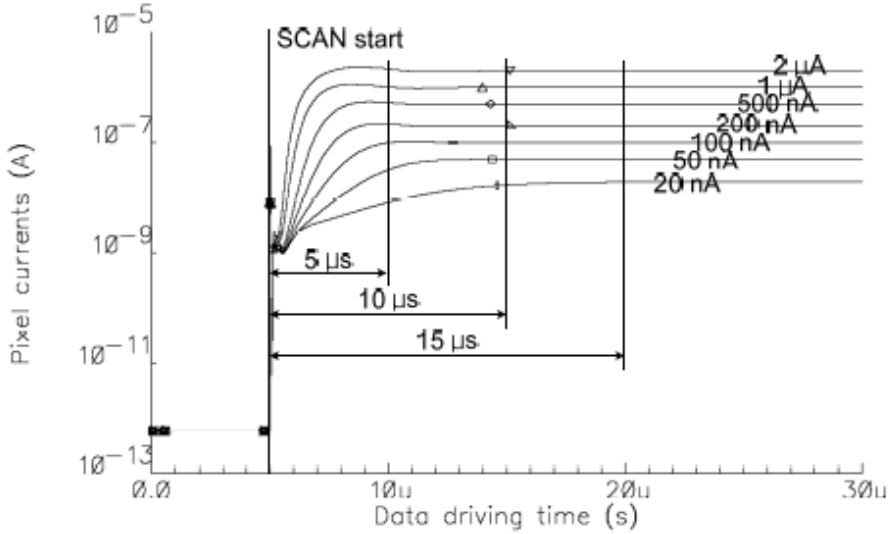


I_{DATA} effects on the loop gain (C_{PP} = 40 pF)

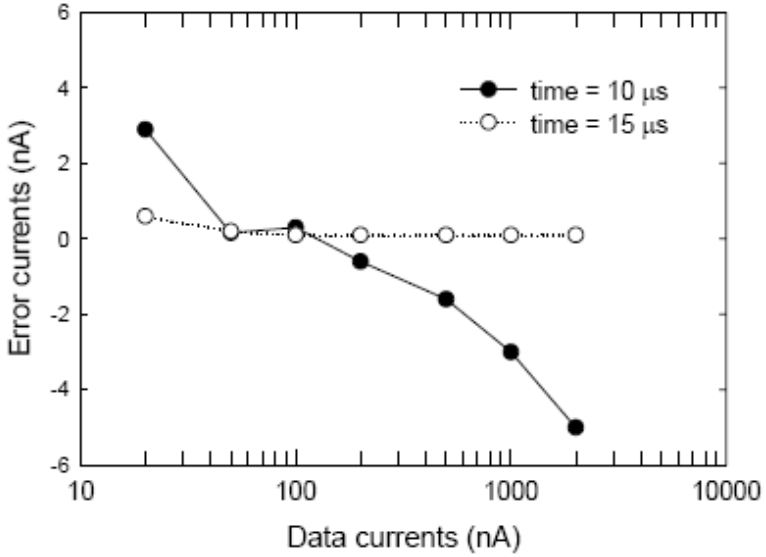
LG < 0dB !!

C_{PP} effects on the loop gain (I_{DATA} = 100 nA)

Driving Speed



Step responses of the TCF driving
(V_{PC} = 300 mV, Load = 6 kohm, 40 pF, SCAN = 5 μs)



10 us of driving time and 5 nA error !!!

Error currents at fixed driving time
(V_{PC} = 300 mV, Load = 6 kohm, 40 pF)

Part III

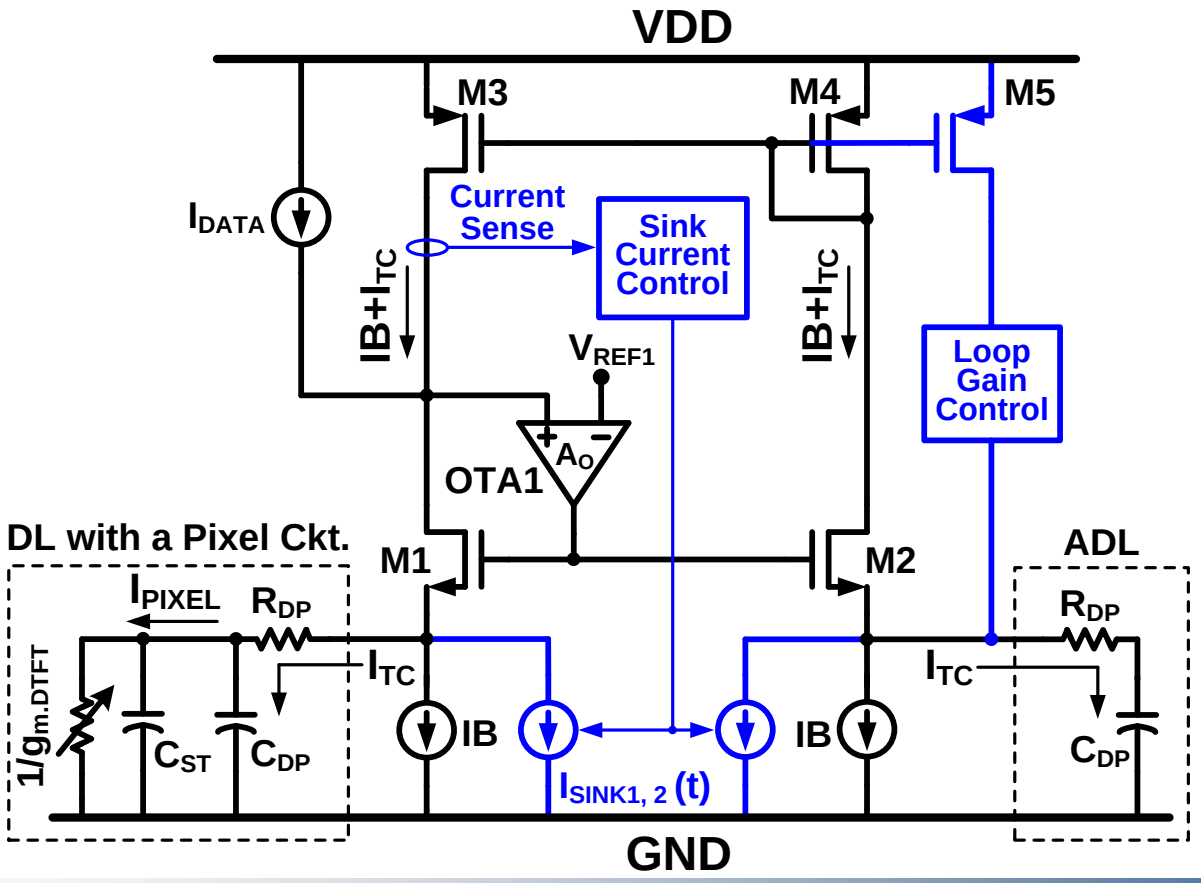
Current-mode AMOLED Drivers:
PP-TCF (Push-Pull Transient Current Feedforward) Driver

PP-TCF Data Driver (1/15)

■ Conceptual Diagram of Push-Pull TCF Driver

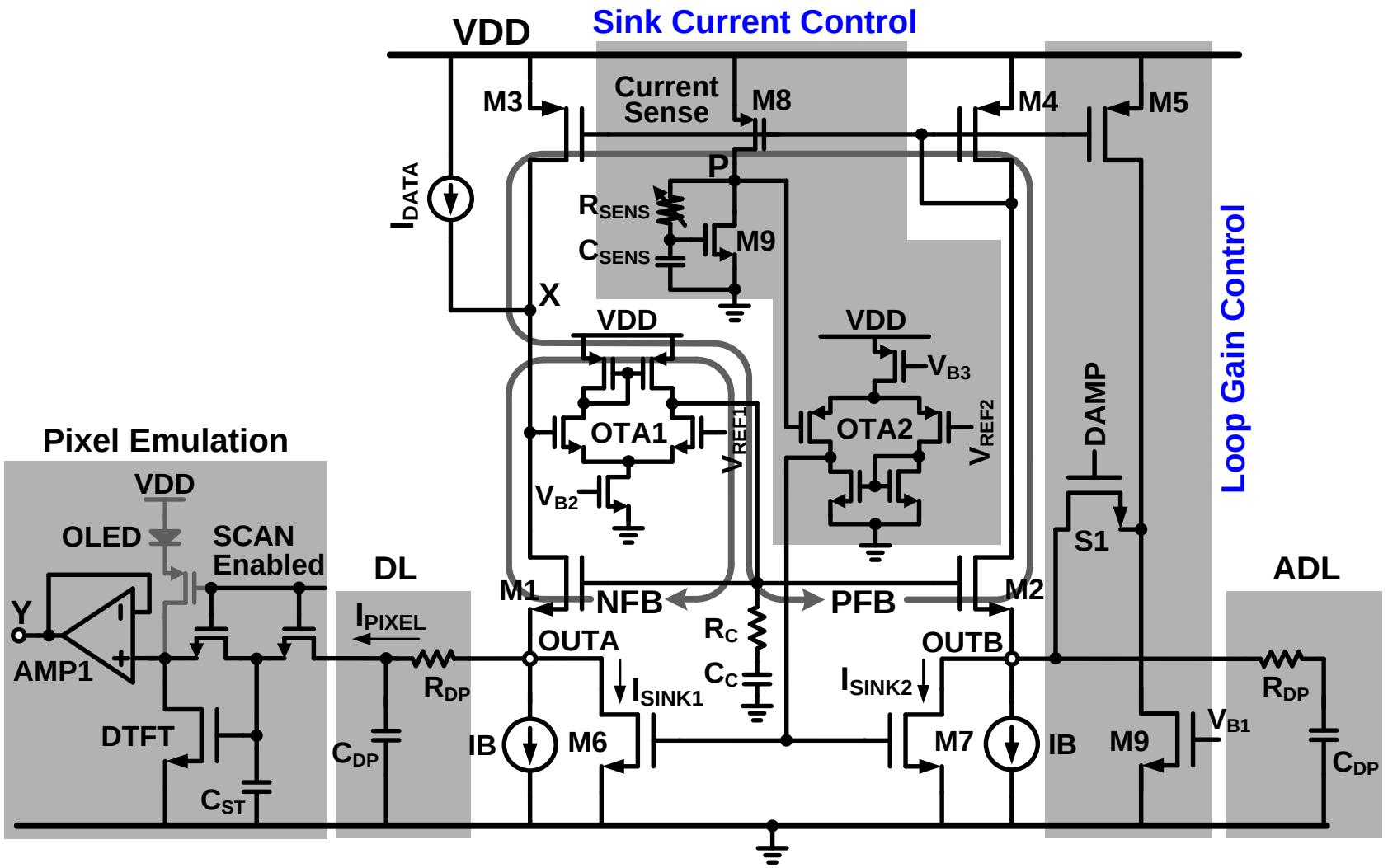
-Complete push-pull function for output currents

-PFB gain control for removing undulation phenomena in pixel currents



PP-TCF Data Driver (2/15)

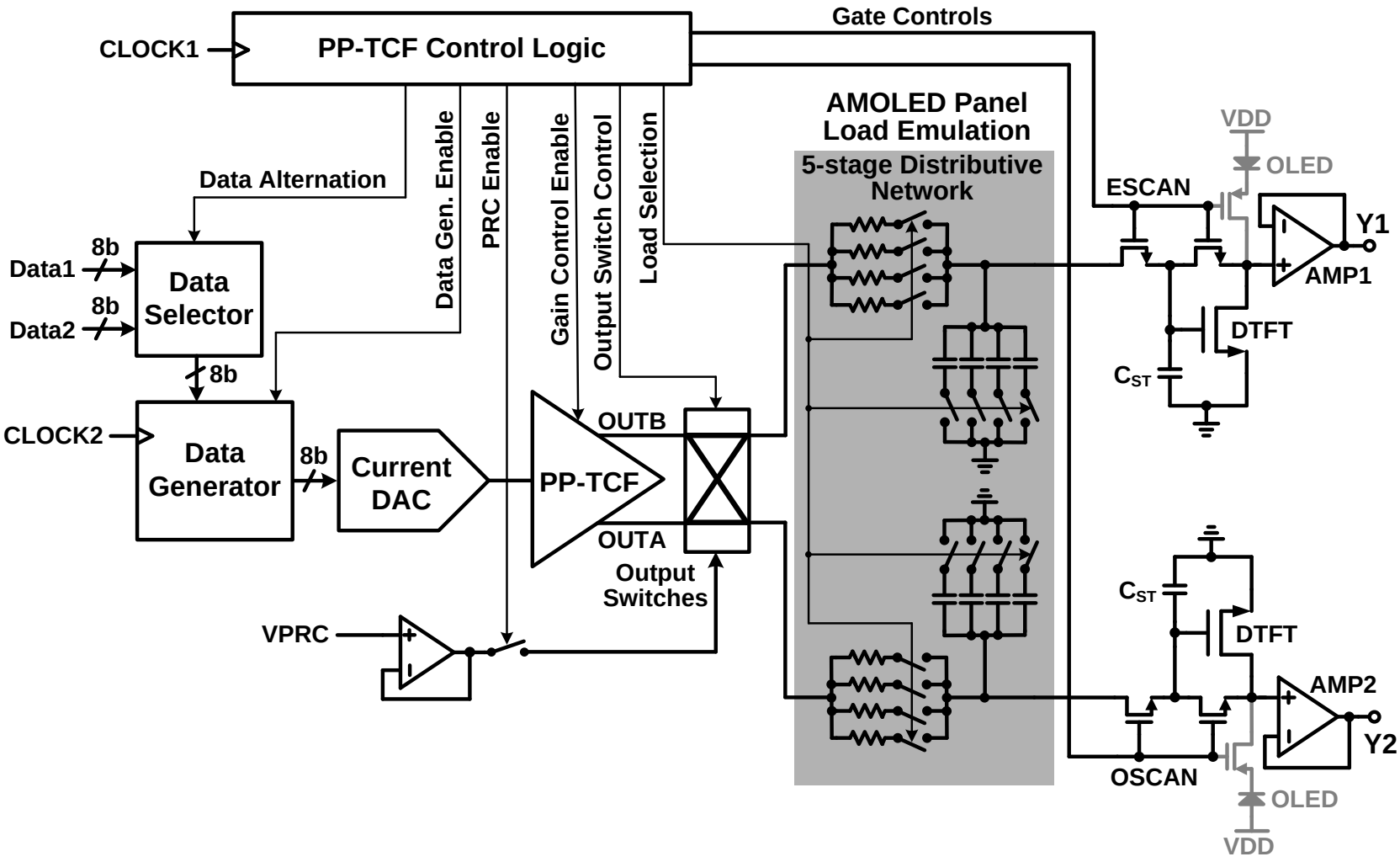
■ Detailed Schematic for PP-TCF Driver



PP-TCF Data Driver (4/15)

■ Functional Diagram of Prototype Driver IC

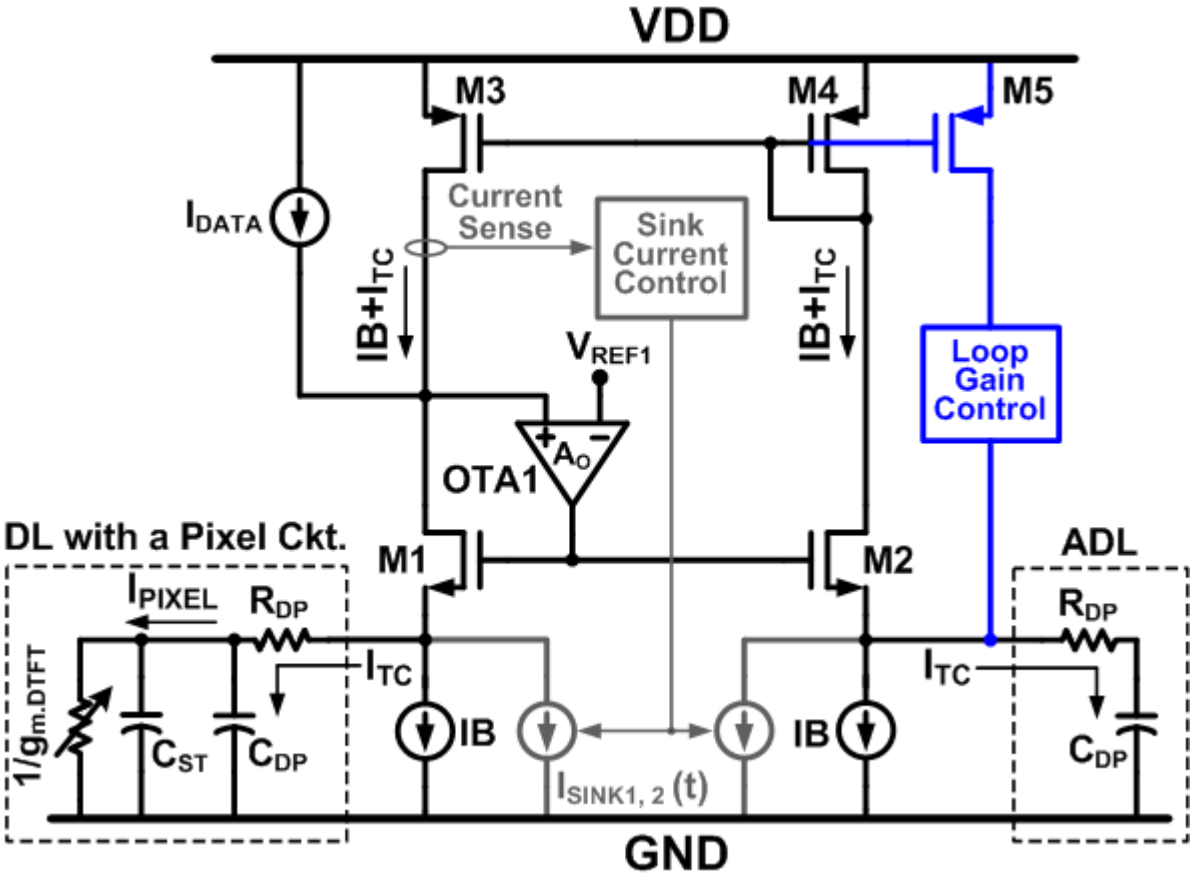
Various functions for evaluating the performances of PP-TCF driver



PP-TCF Data Driver (5/15)

■ Positive Feedback Loop (PFB) Gain Control (1)

PFB gain control for removing undulation phenomena in pixel currents

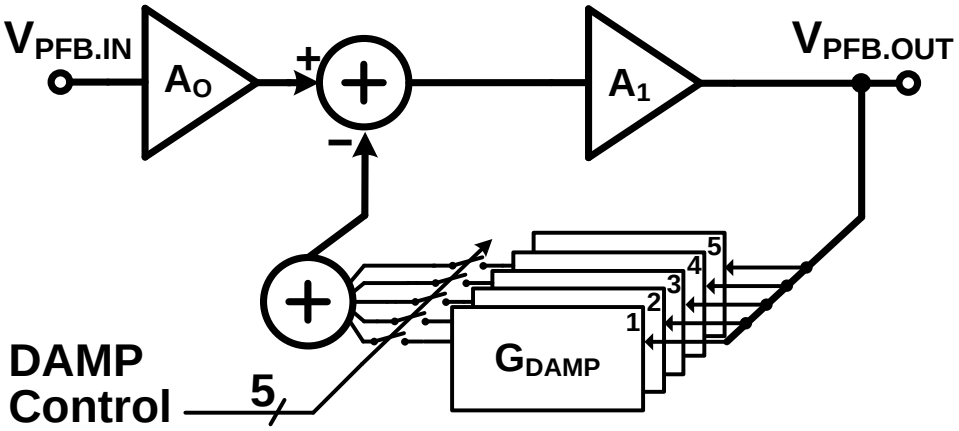


PP-TCF Data Driver (6/15)

■ Positive Feedback Loop (PFB) Gain Control (2)

PFB gain control for enhancing pixel current settling (IDATA= 3uA, panel parasitic 2kOhm/ 60pF)

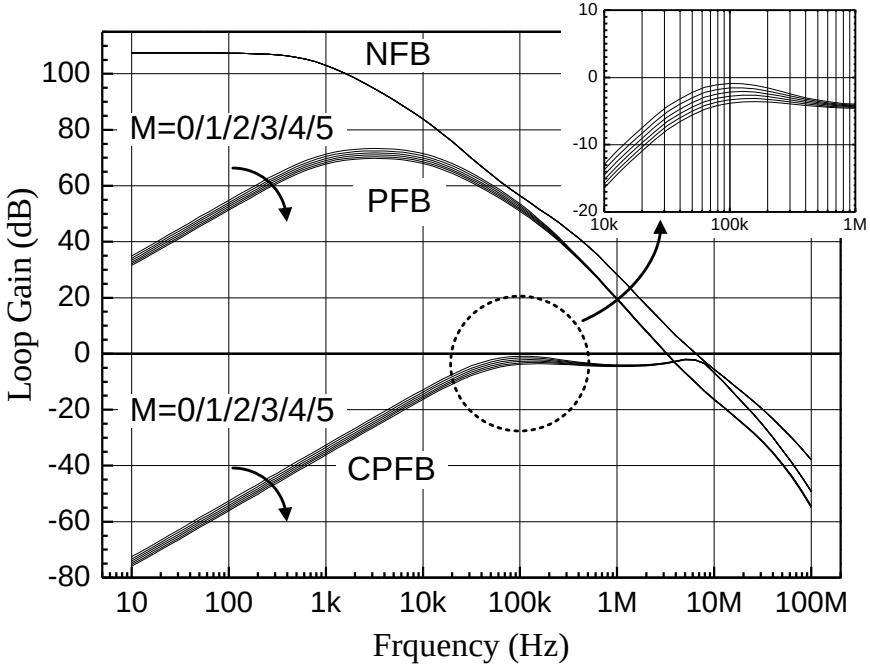
Conceptual Diagram for PFB Gain Control



$$A_{PFB.DAMP} = A_O \times \frac{A_1}{1 + M \cdot G_{DAMP} \cdot A_1}$$

$$= \frac{A_{PFB}}{1 + M \cdot G_{DAMP} \cdot A_1}$$

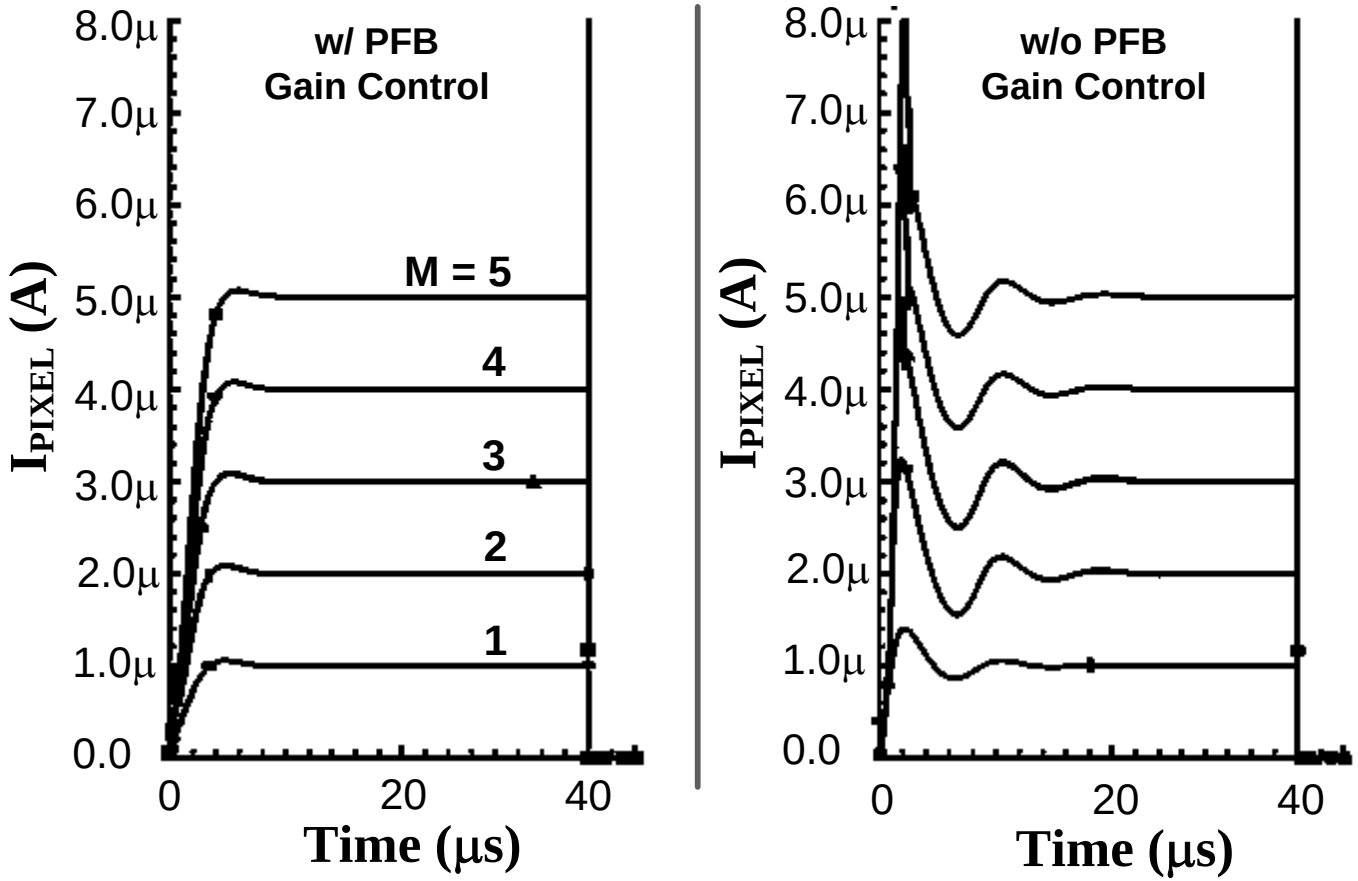
Simulation Results



PP-TCF Data Driver (7/15)

■ Positive Feedback Loop (PFB) Gain Control (3)

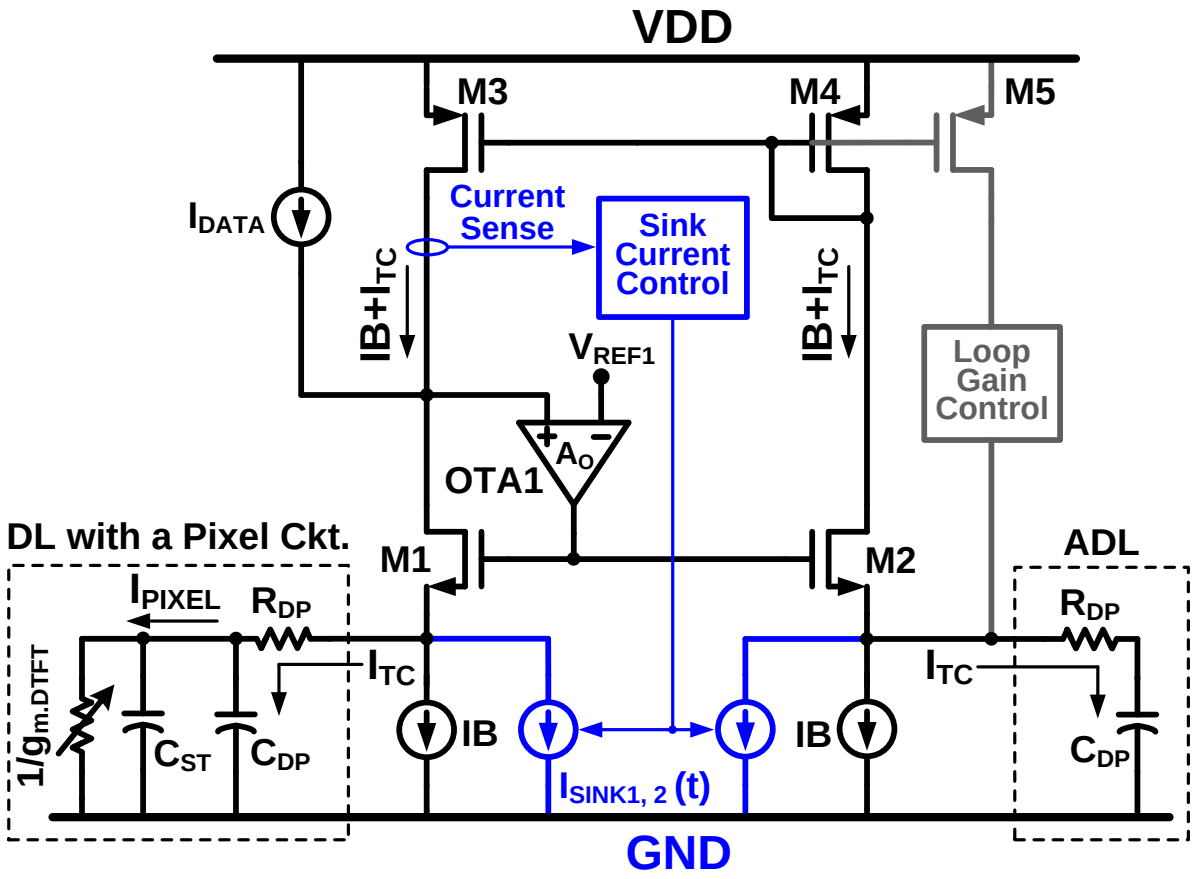
Simulated driving waveforms with/ without PFB gain control (IDATA= 1 to 5uA, panel parasitic 2kOhm/ 60pF)



PP-TCF Data Driver (8/15)

■ **Current Pulling Function for Enhancing Data Current Settlement (1)**

Complete push-pull function for output currents

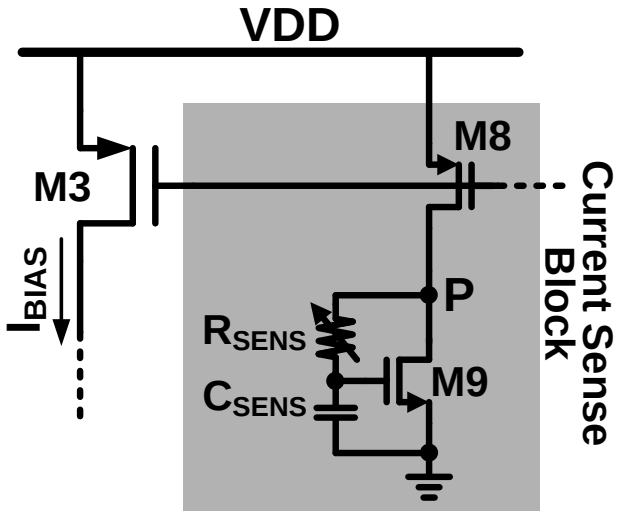


PP-TCF Data Driver (9/15)

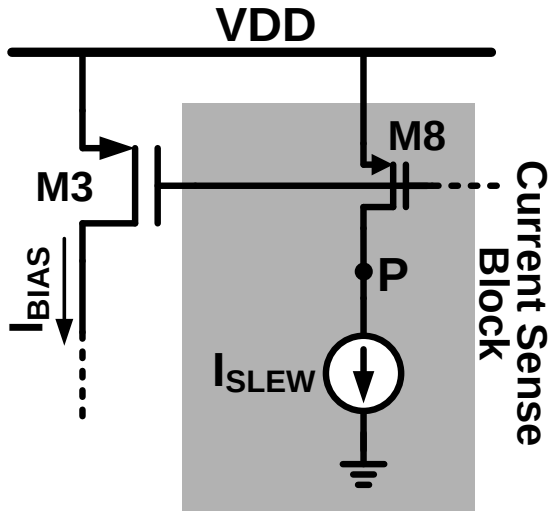
■ Current Pulling Function for Enhancing Data Current Settlement (2)

Fast current sense block for current pulling operation

Fast Current Sense Circuit



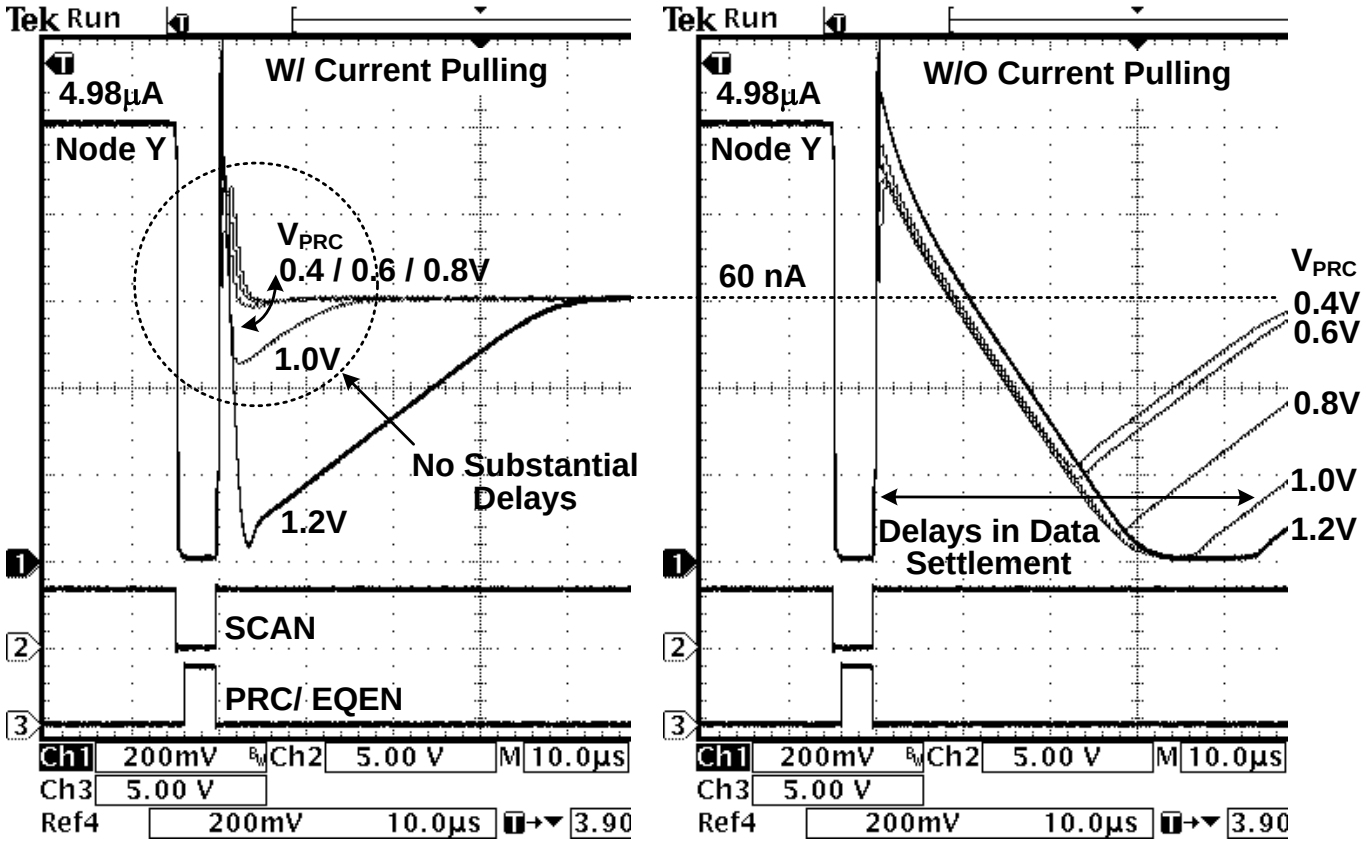
Conv. Current Sense Circuit



PP-TCF Data Driver (12/15)

■ Measurement results (1)

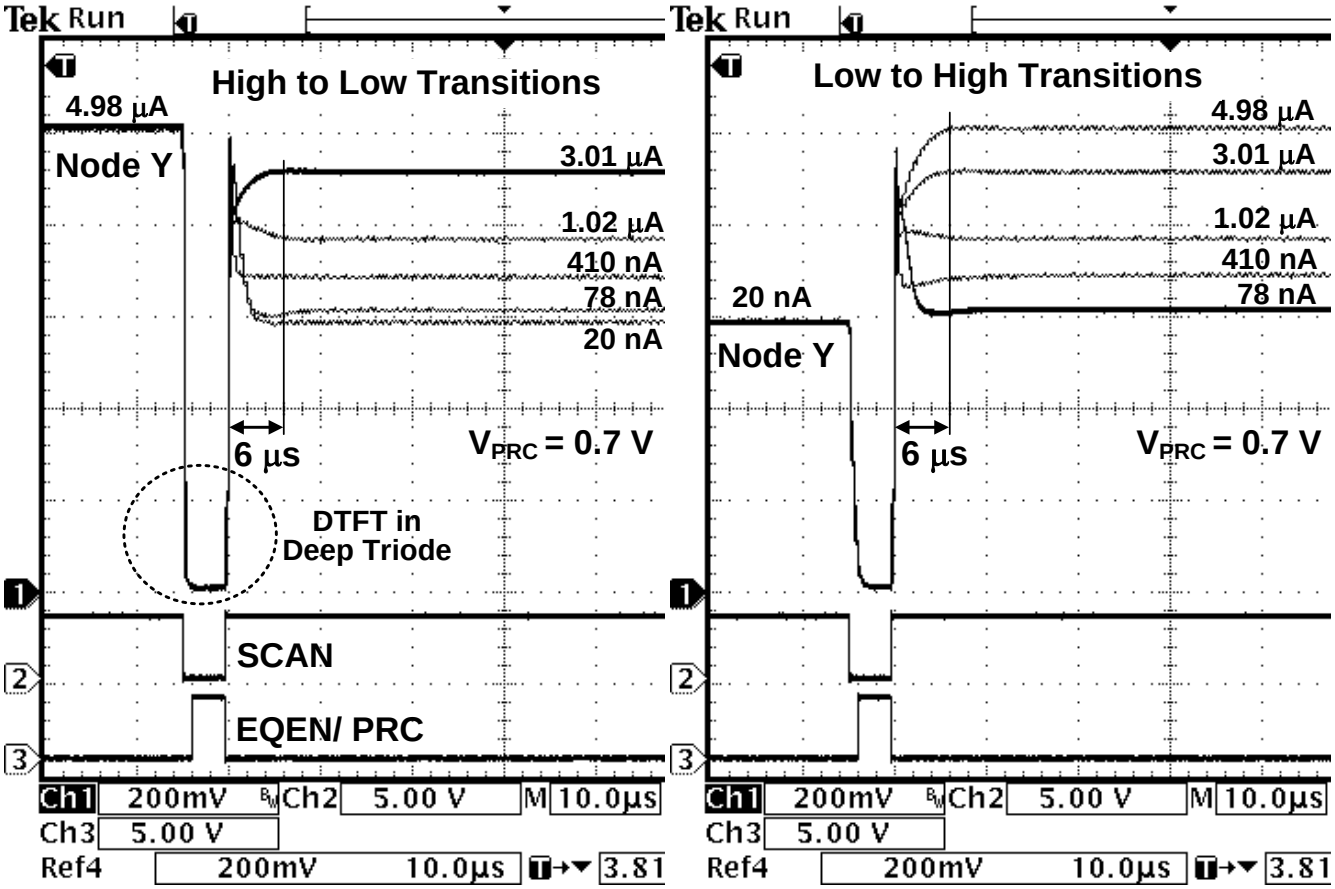
Pixel current settling times improved by current pulling function (IDATA transitions from 4.98uA to 60nA, VPRC= 0.4 to 1.2V, 0.2V step, panel parasitic 4kOhm/ 90pF)



PP-TCF Data Driver (14/15)

■ Measurement results (3)

Waveforms for various data current levels: High to low transitions and low to high transitions of data currents (data current = 20nA to 4.98uA, V_{PRC}= 0.7V, parasitic load = 4kOhm/ 90pF)



PP-TCF Data Driver (15/15)

■ Performance summary

Process	0.35 μm CMOS (1P 4M)
Operation voltage	3.3 V
Data current range	20 nA to 4.98 μA
Gray scale	8 bit (16.8 million colors)
Maximum driving load (Panel parasitics)	4 kΩ / 90 pF (Full-HD)
Settling time	≤ 6 μs
Static current	4.5 μA / Channel
Occupation area	60 × 308 μm^2 / 2 Channels

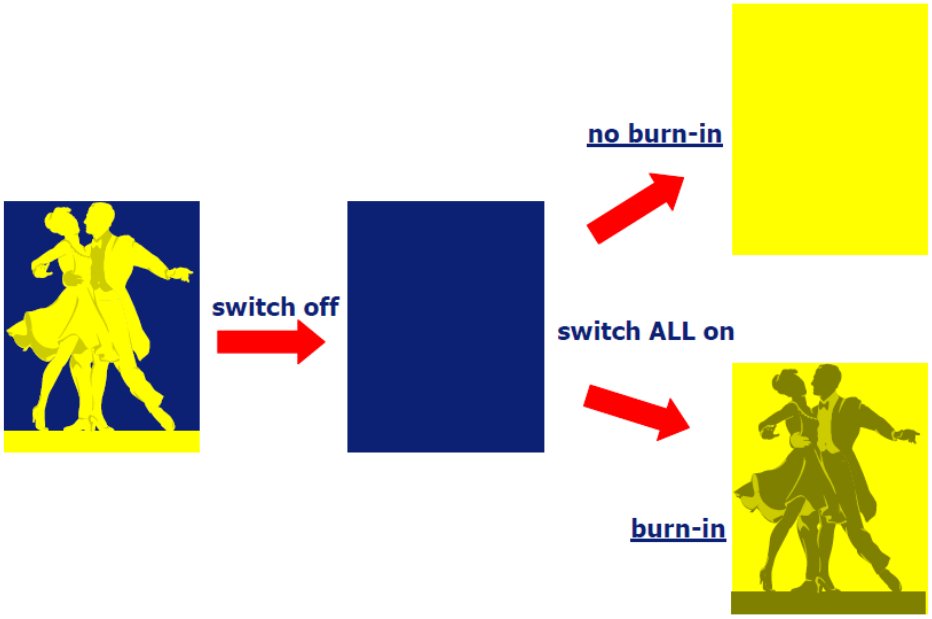
❒ **Appropriate for FHD AMOLED displays**
- **Low power consumption**
- **Stable operation at high data currents**

Part IV

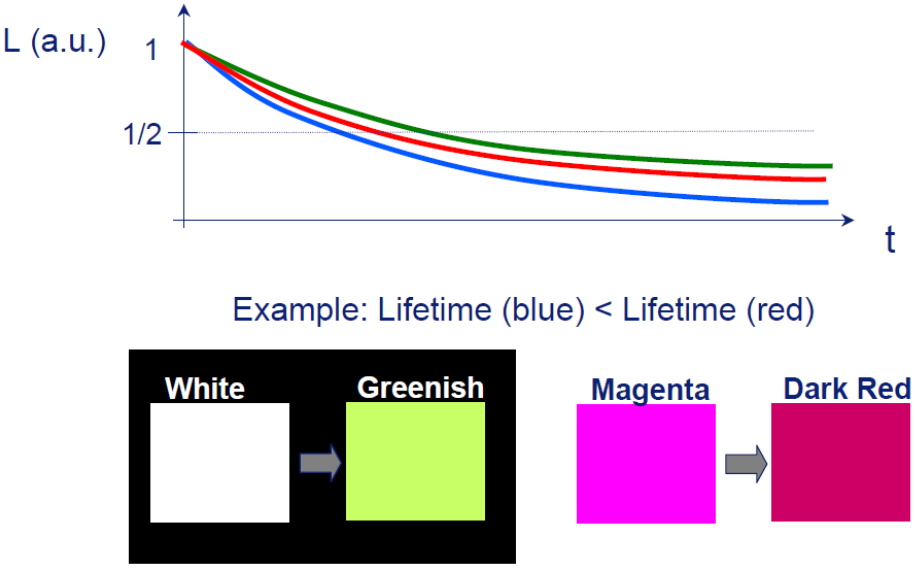
Real-time Image Sticking Compensation using Current Driving

OLED Degradation

Burn-in

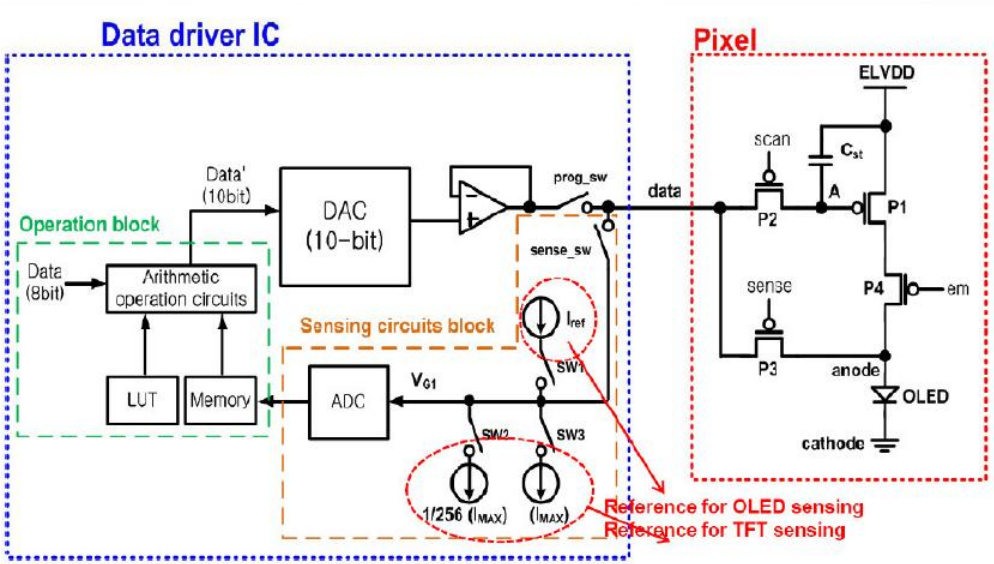


Discoloration



- **Differential aging dependent on sub-pixel.**
- **Prolonged display of static image (burn-in)**
- **RGB have different degradation curves.**

Conventional Image Sticking Compensation



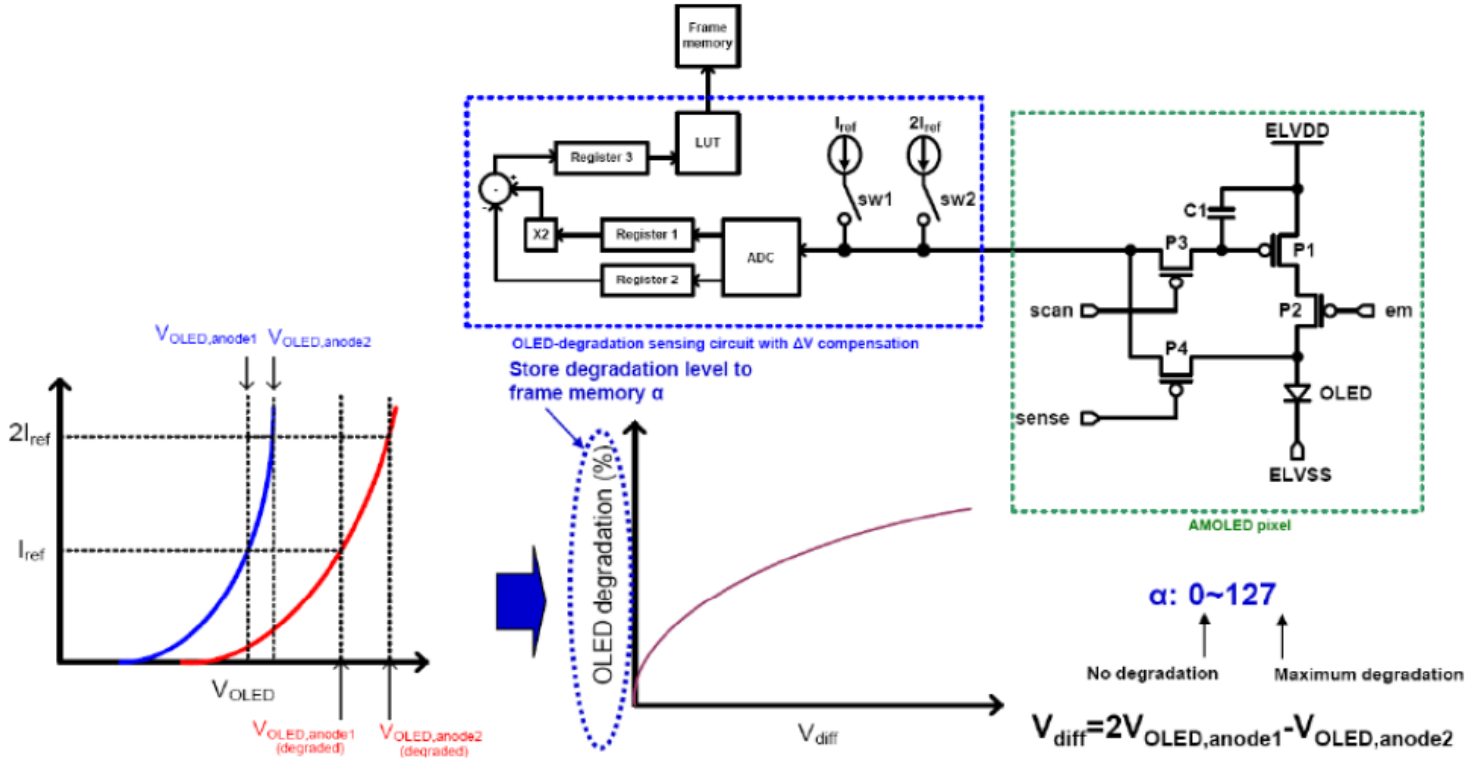
<기존 전압 구동용 IS 보상회로>

✓ TFT variation 문제를 해결하더라도, OLED 소자 자체의 시변 열화 특성으로 인해 잔상(Image Sticking)효과를 유발.

✓ OLED의 양단 전압이 열화에 따라 증가하는 현상을 이용한 Electrical Feedback 방식이 연구되고 있음.

✓ 기존 연구 방식들은 모두 전압 구동용 보상회로

OLED Degradation Sensing



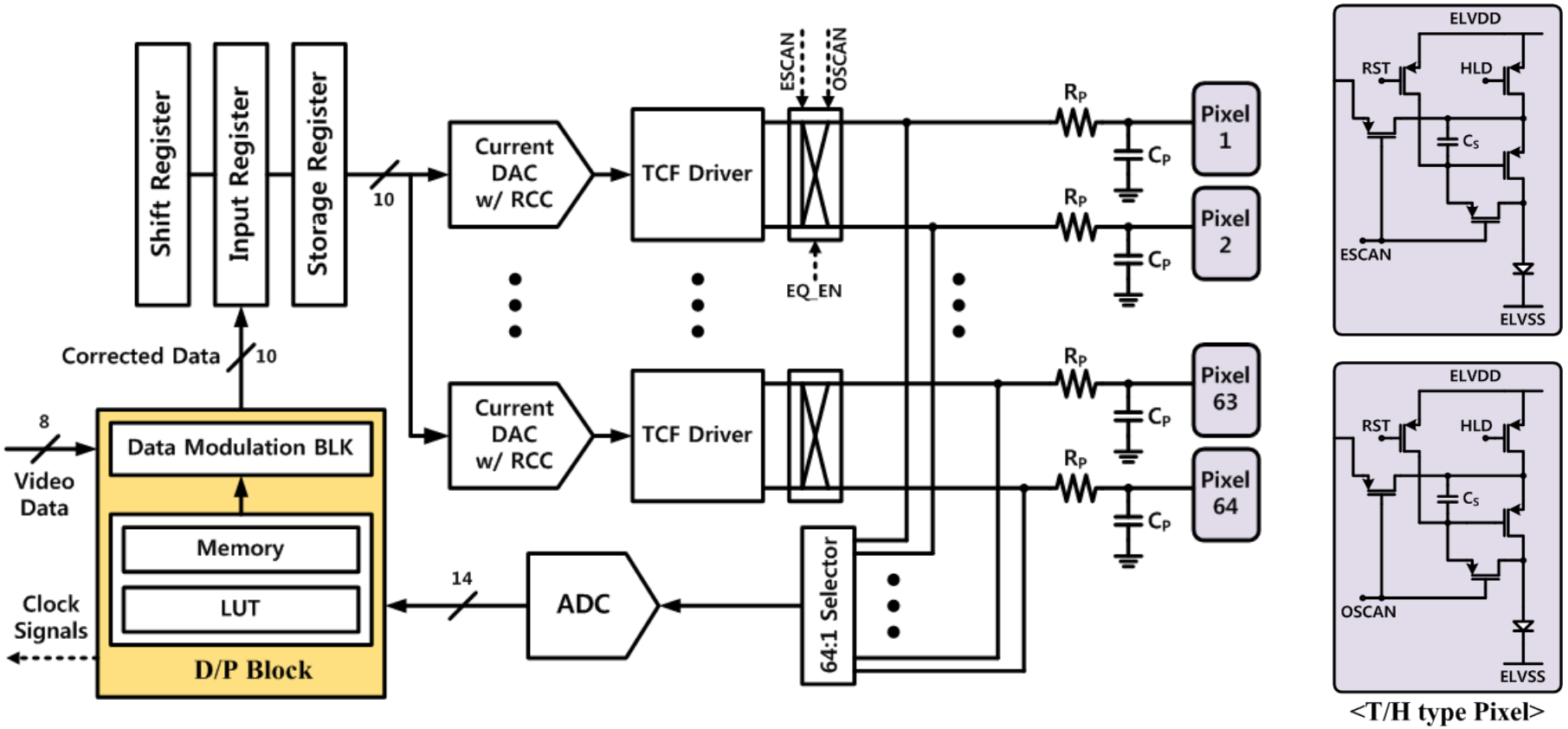
<OLED degradation Sensing>

Real-time Compensation using Current Driving (2/7)

■ IS 보상 방식 비교

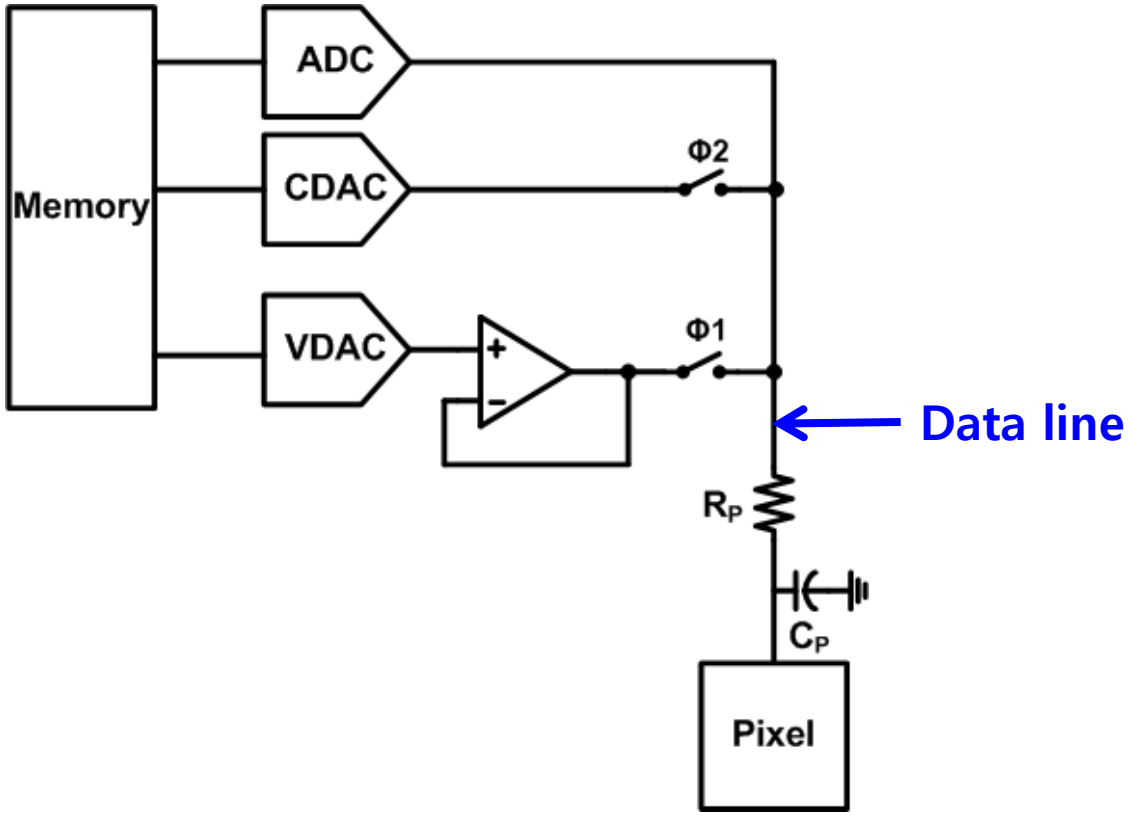
	Compensation Method using Voltage Driving	Real-time Compensation using Current Driving
보상전류	별도의 큰 전류	작은 데이터 전류
열화 가속	Fast	Slow
메모리 크기	Large (Vth, μ, OLED)	기존의 1/3 이상 감소 (OLED)
보상시간	Long time	Real time

Real-time Compensation using Current Driving (3/7)



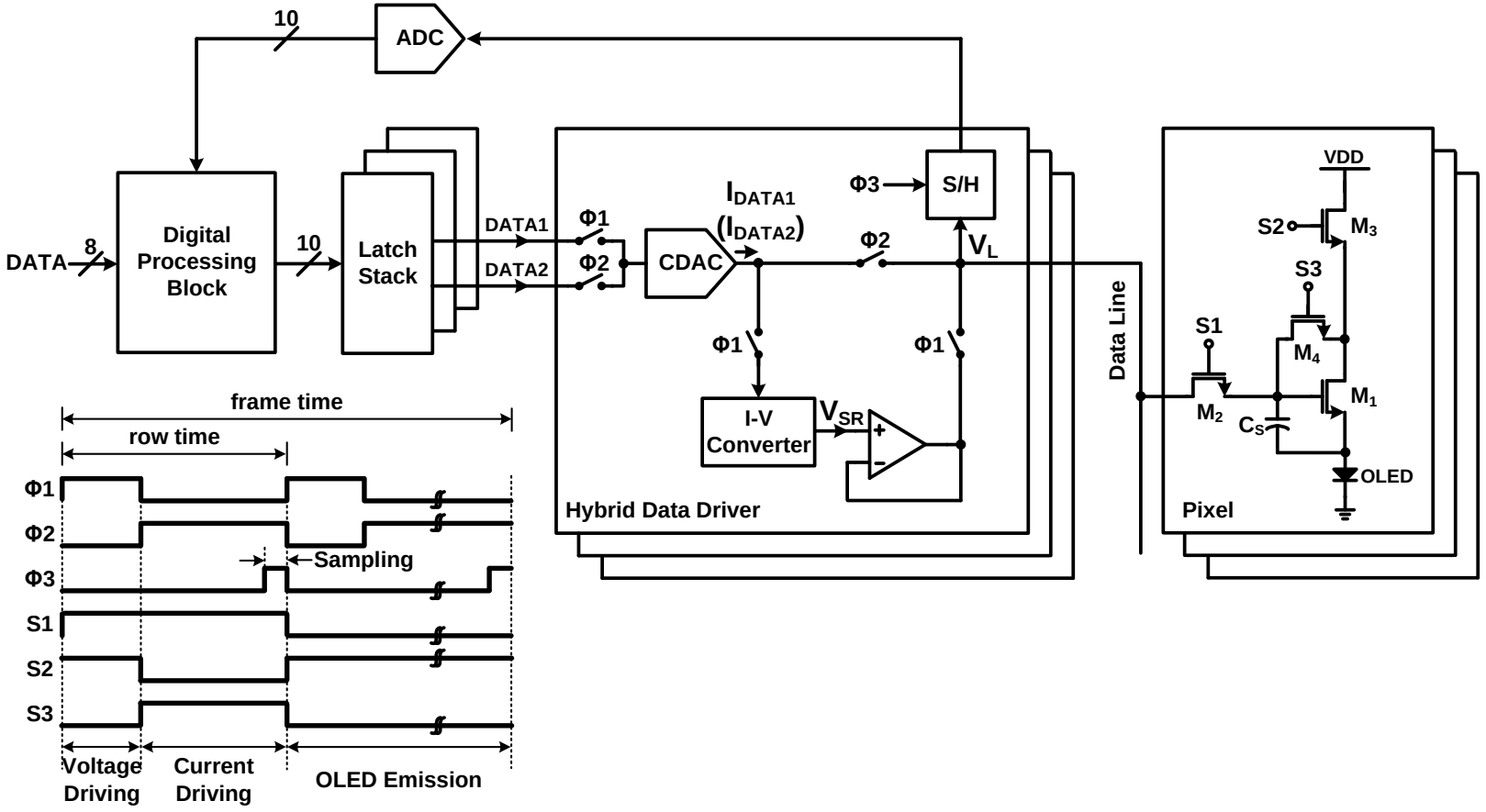
- 1:2 DeMUX operation
- Track and Hold type pixel
- TCF driver
- Current DAC with Reference Current Calibrator

Hybrid Data Driver



1. Read data-line voltage by ADC (OLED compensation)
2. Store by line voltage information of each pixel at memory
3. ϕ1, VDAC & Amp. pre-charge data-line by pre-stored information.
4. ϕ2, CDAC provides data current to pixel. (TFT compensation)

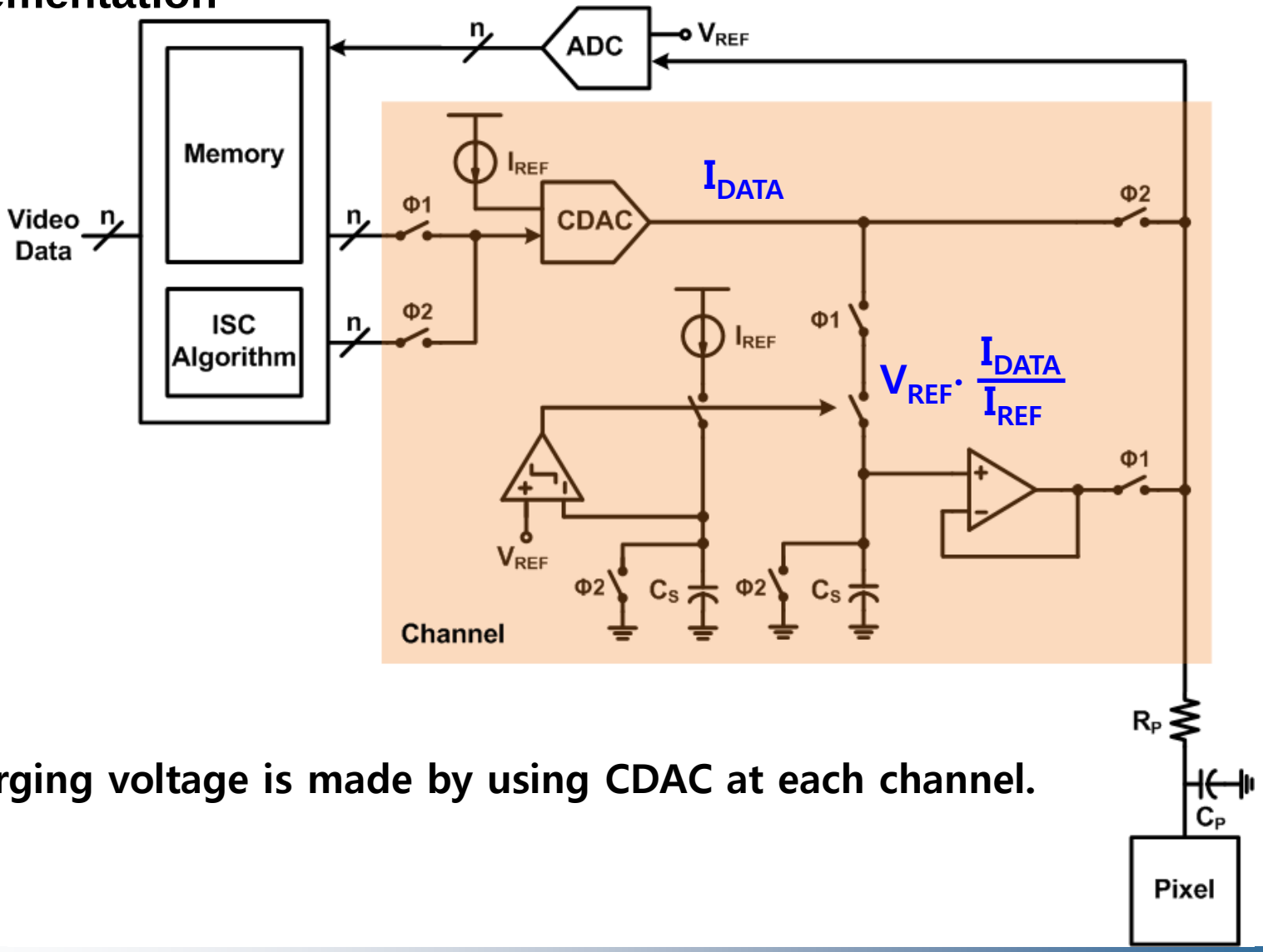
Block Diagram of Hybrid Data Driver



- **CDAC sharing scheme**
- **VDAC = CDAC + I-V Converter**
- **DATA1 for voltage driving, DATA2 for current driving**

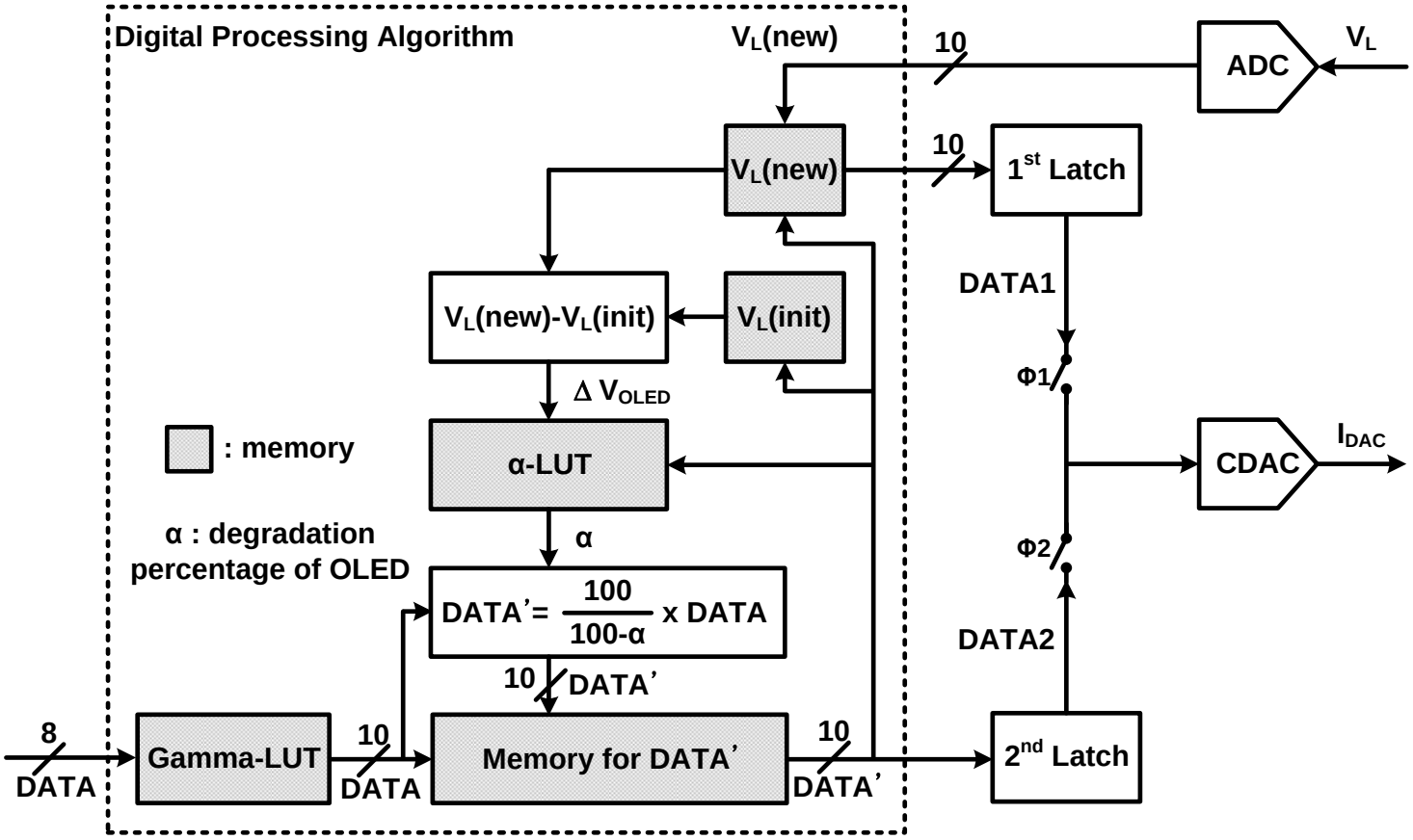
Real-time Compensation using Dual Data Driving (3/4)

■ Implementation



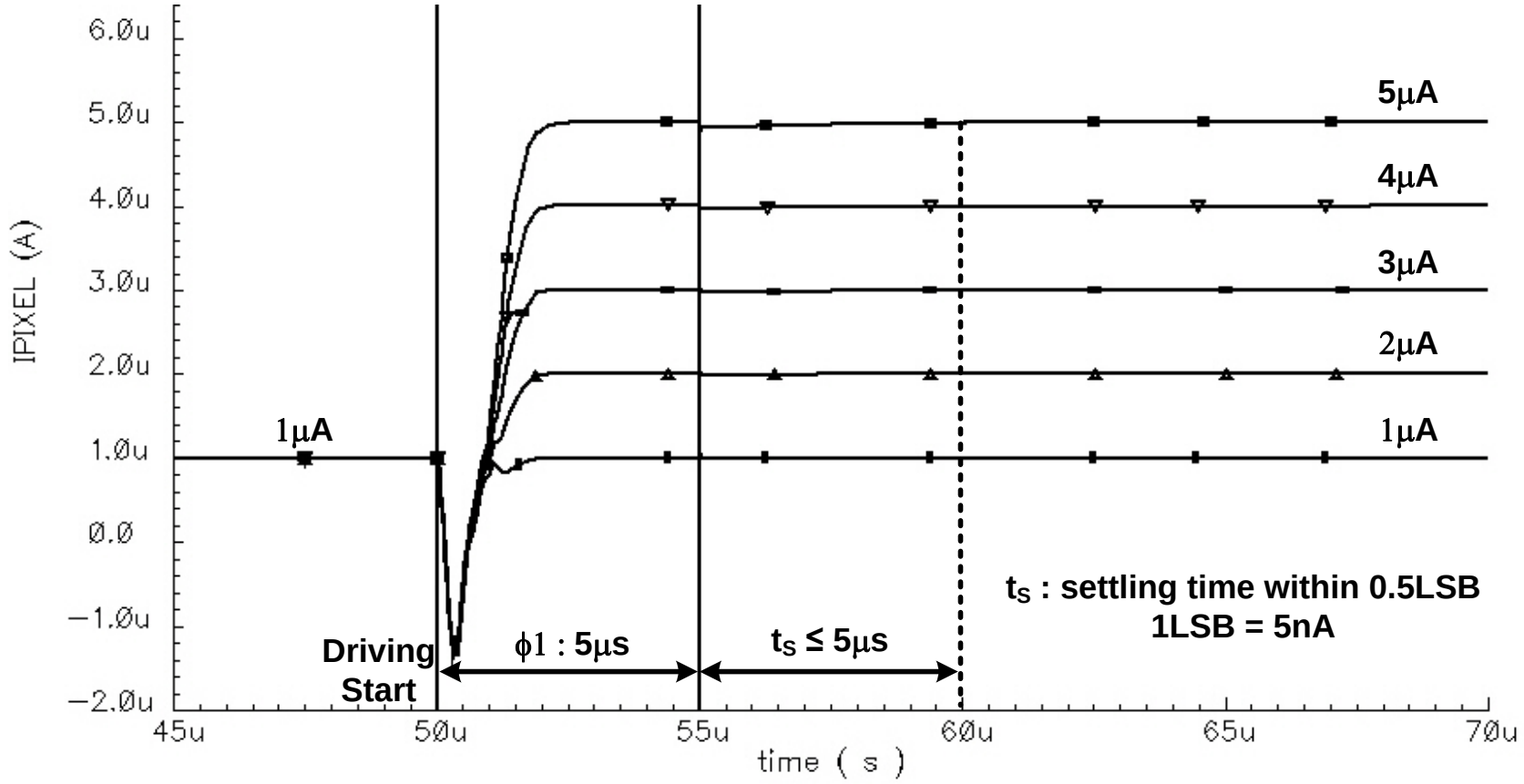
✓ Pre-charging voltage is made by using CDAC at each channel.

Digital Processing Algorithm



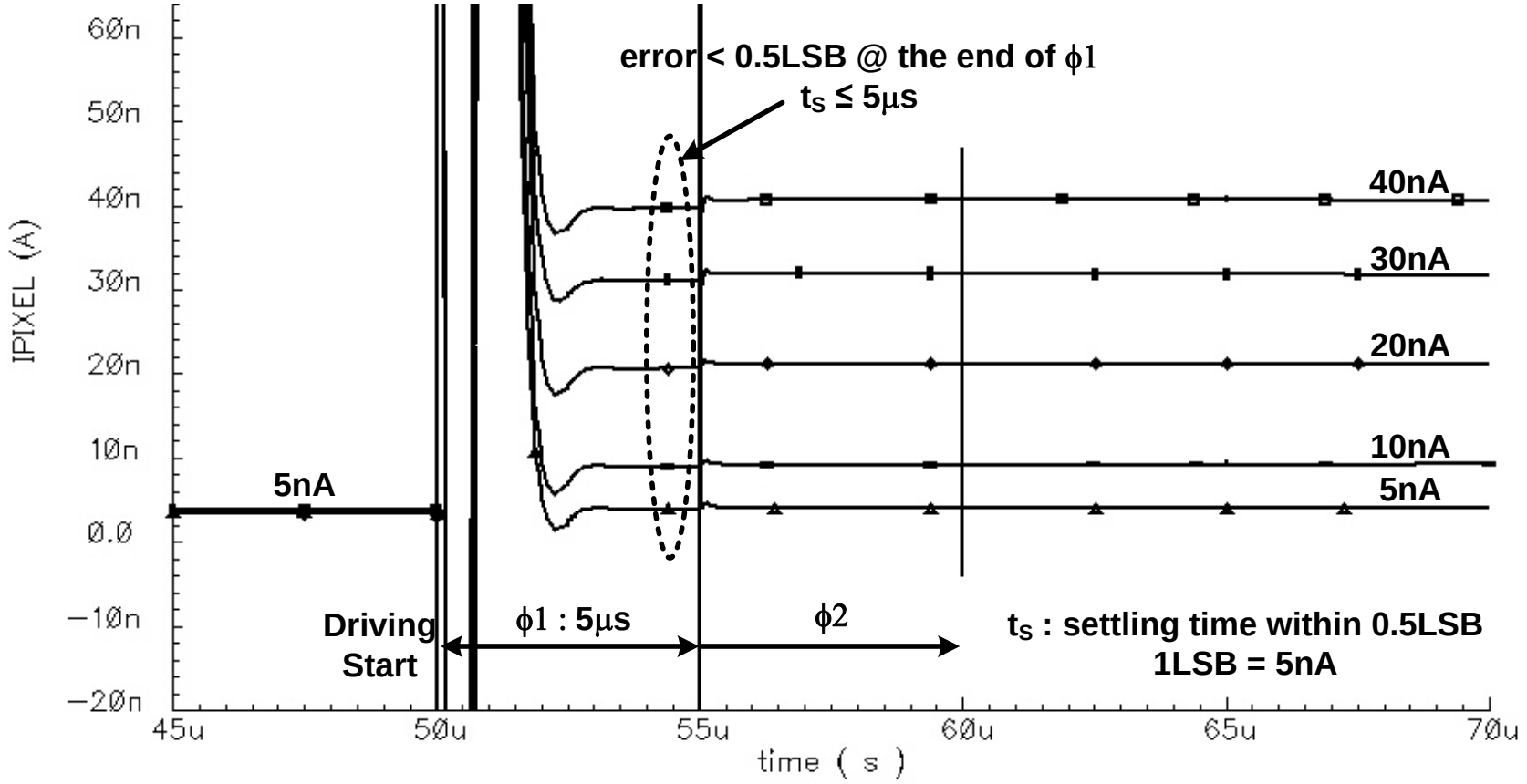
- **DATA1 and DATA2 for hybrid data driving**
- **α-LUT for OLED compensation**

Data Transition



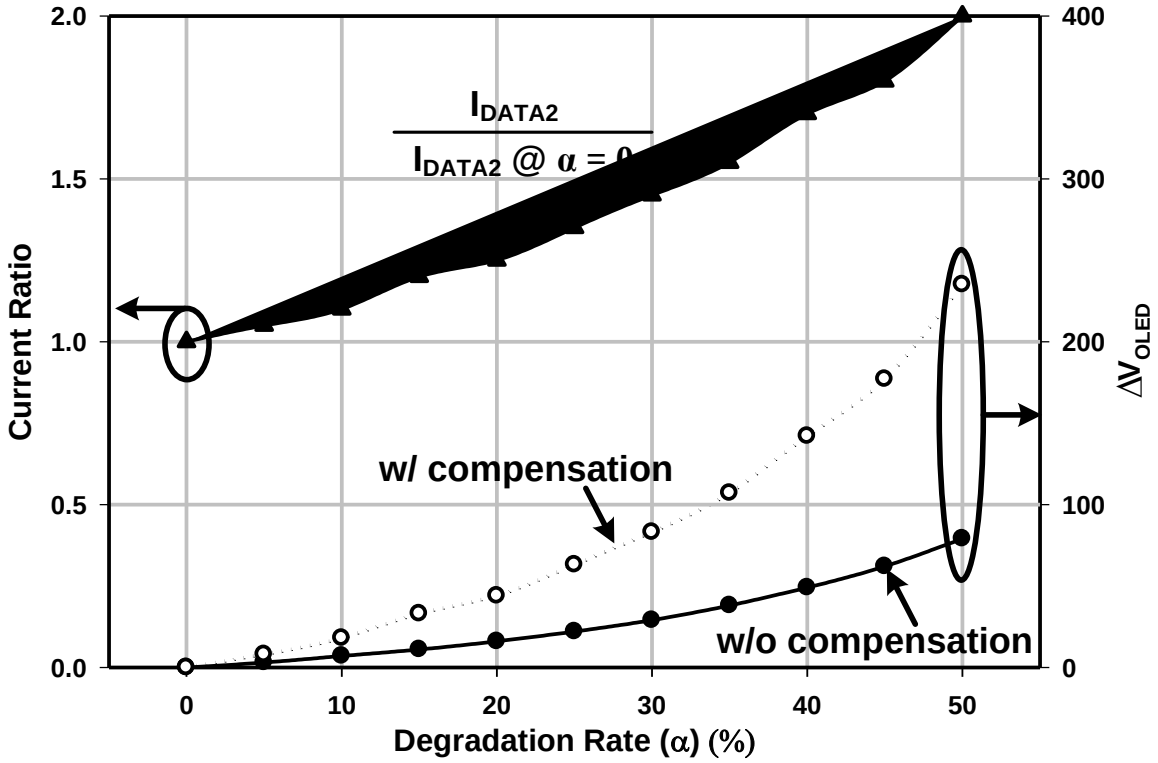
- **Data driving waveforms for various current levels**
- **High current level (1uA~ 5uA, 1uA step)**

Data Transition



- **Data driving waveforms for various current levels**
- **Low current level (5nA~ 40nA)**

Parameter Variation with Degradation Rate



- **Changes of I_{DATA2} and ΔV_{OLED} by compensation algorithm**
- **I_{DATA2} @ α=0% =100nA**

Summary

- **Feedback (DFFC) driver**
  - ✓ Range of data currents from 10nA to 2.55uA
  - ✓ WXGA-sized panel load of 1.5kOhm/ 100pF.

- **Feedforward (TCF, ITCF, PP-TCF) drivers**
  - ✓ Full range of data currents from sub-10nA to 5μA
  - ✓ Various panel load condition from XGA to FHD-sized panel

- **Real-time image sticking compensation methods**
  - ✓ Compensate the luminance degradation of OLEDs
  - ✓ Compensate the variation of the driving TFT by current driving

PMIC

Single-Inductor Multiple-Output (SIMO) DC-DC Converters

KAIST

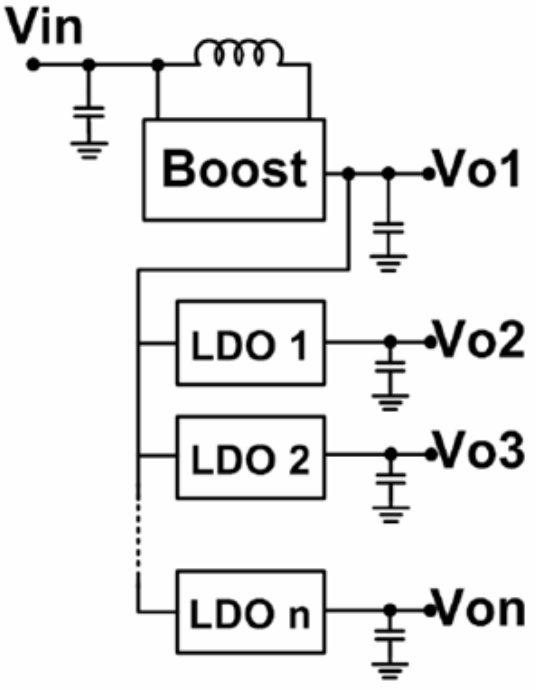
Dept. of EECS,
Circuit Design & System Application Laboratory

Motivation (1)

Why Multiple On-Chip supply ?

- Different blocks require different supplies
- AMOLED display requires multiple supplies
- Voltage Scheduling scheme for effective power saving in digital circuit
- Performance improvement in analog & mixed signal systems

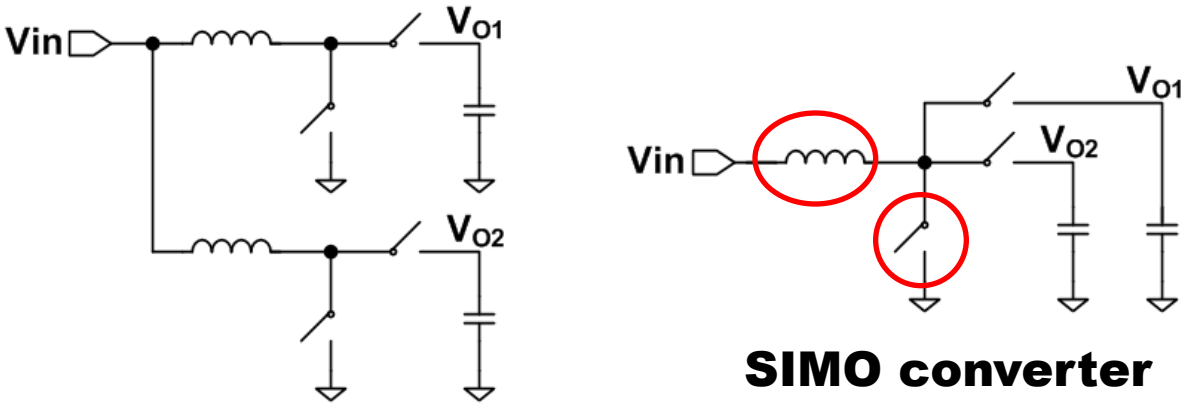
Background (1) – Boost converter and LDOs



- Advantages
  - Simple
  - Low ripple
  - Short time-to-market
- Disadvantages
  - Voltage drop → Low efficiency

Motivation (2)

Why SIMO converter ?

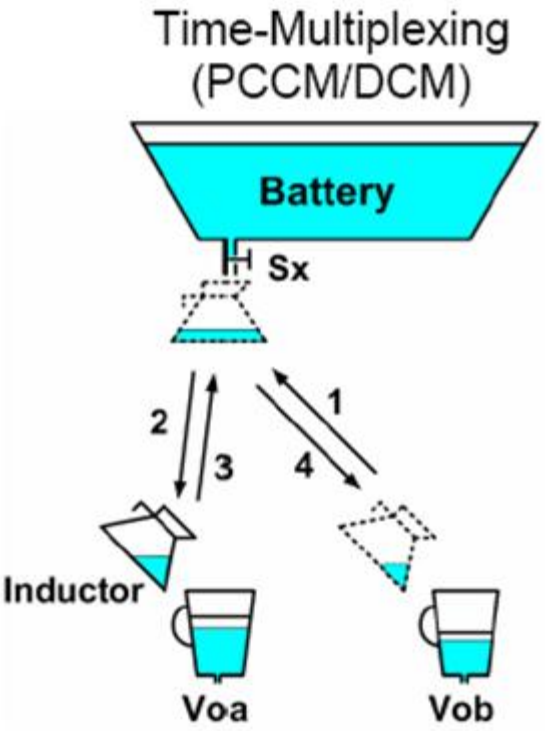


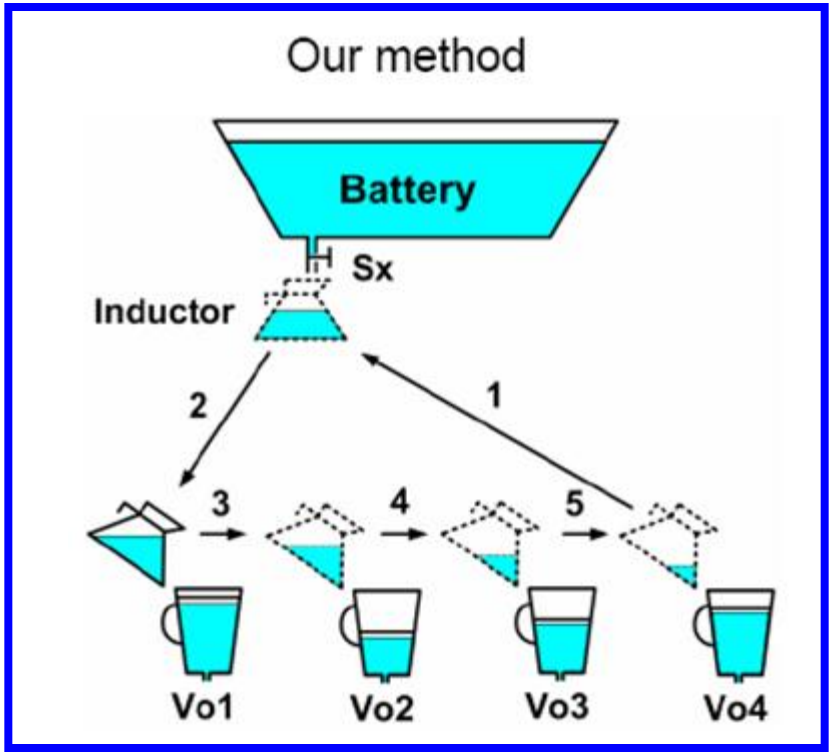
SIMO converter

- Single inductor : fewer magnetic components, fewer IC pins, lower cost, higher integration
- Fewer on-chip power devices

➔ **SIMO converter is a cost-effective solution !!**

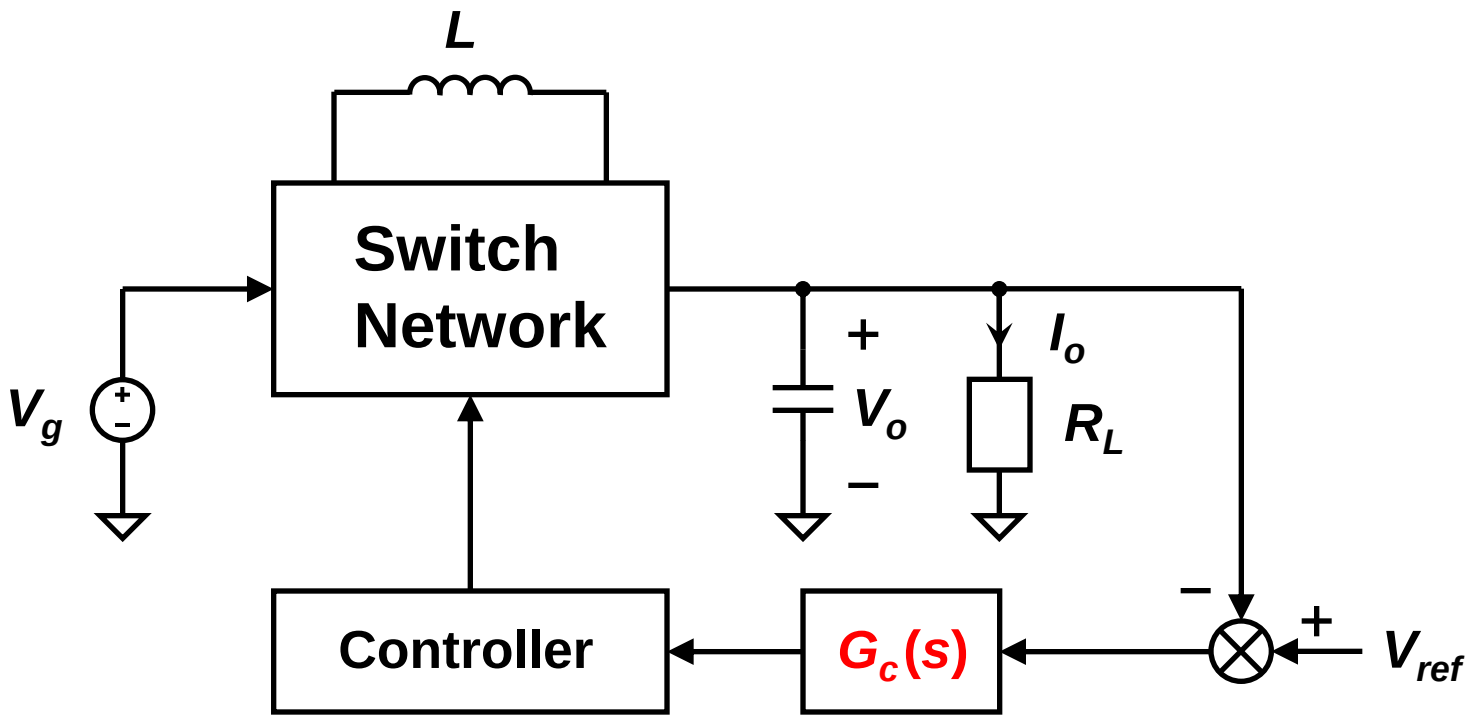
1) Concept of Proposed OPDC





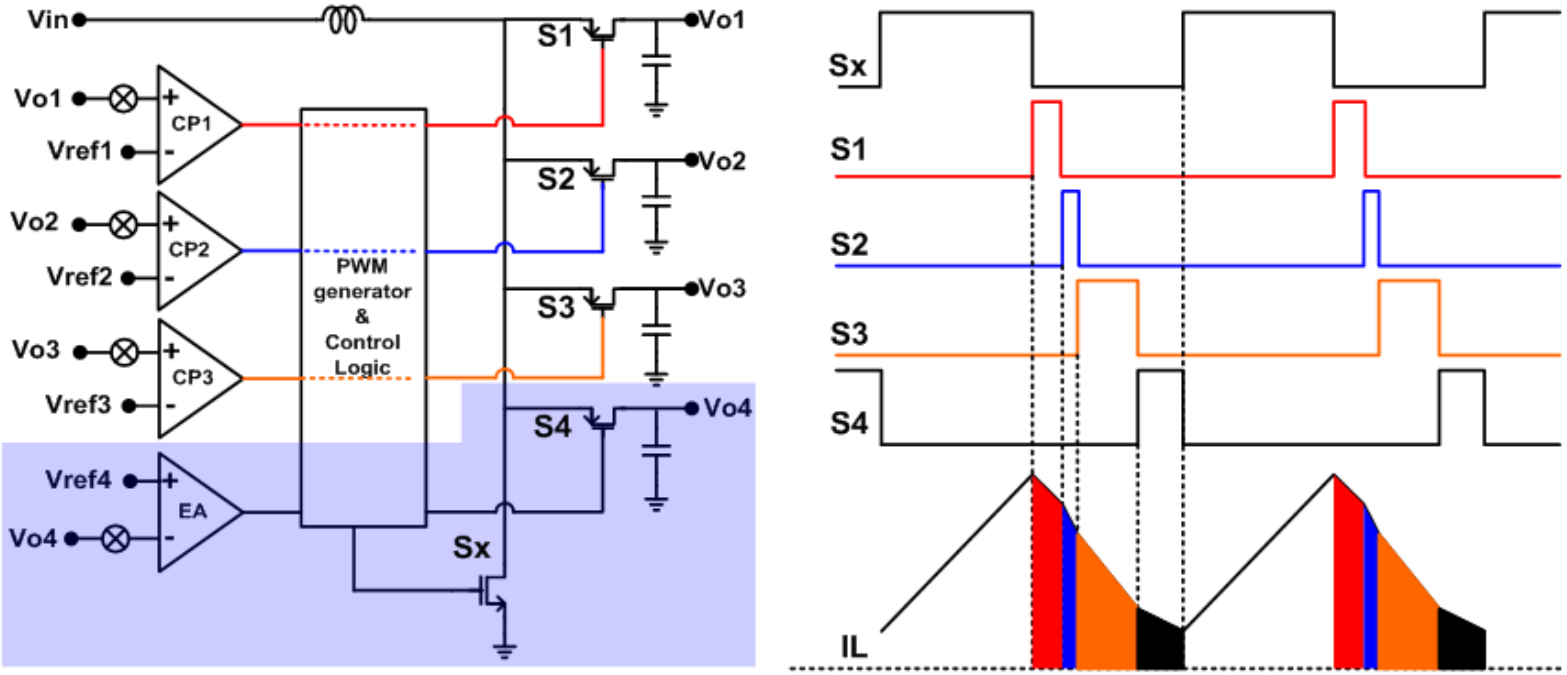
	PCCM/DCM	OPDC
energy transfer per 1 switching cycle	1 per 1	All per 1
# PI compensator	# outputs	1
Output extension	difficult	easy

Existing PWM DC/DC Converters



- Output Voltage Feedback
- Output Cap. and I_O affect the Loop Response
- Compensator Design is NOT EASY

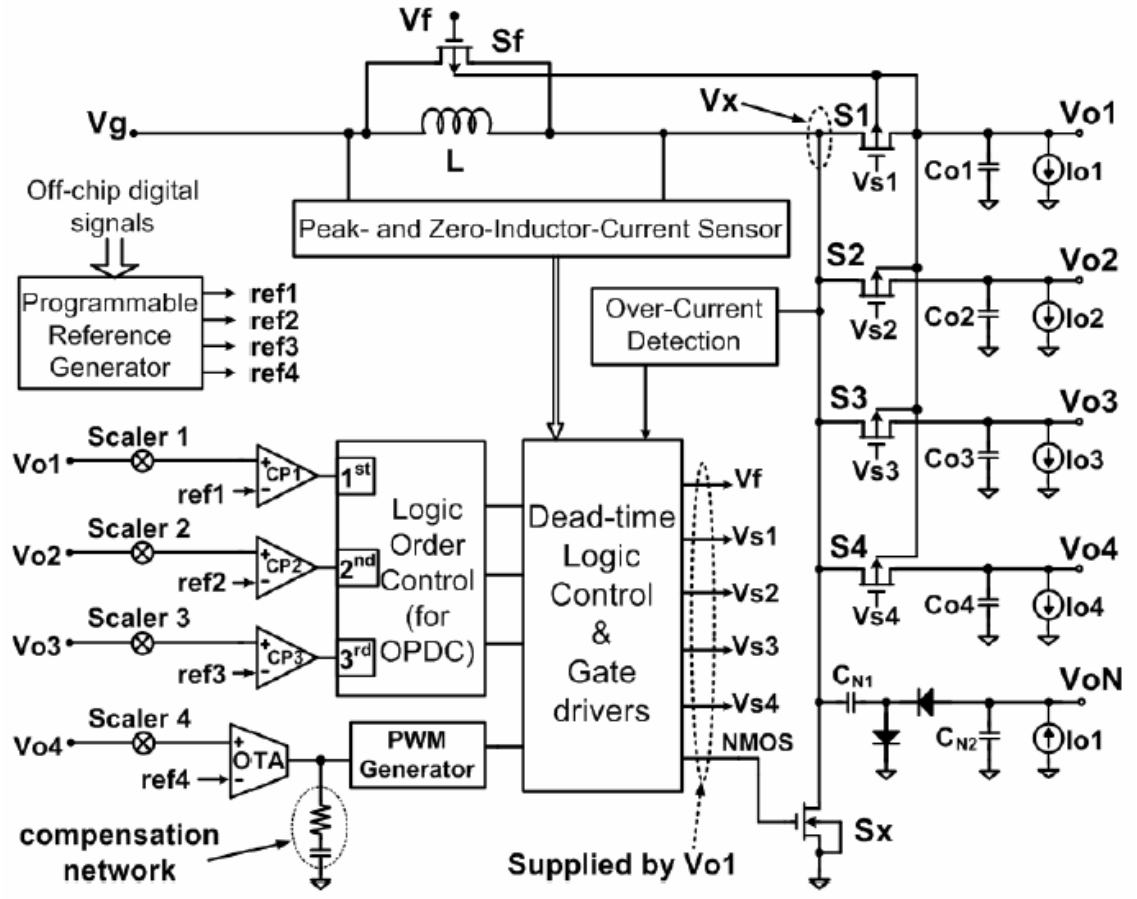
SIMO converter with OPDC



[Phuc.ISSCC2007, JSSC 2008]

- Comparator control method
- Only one PWM controller
- Easy output extension and high power capacity

SIMO converter with OPDC

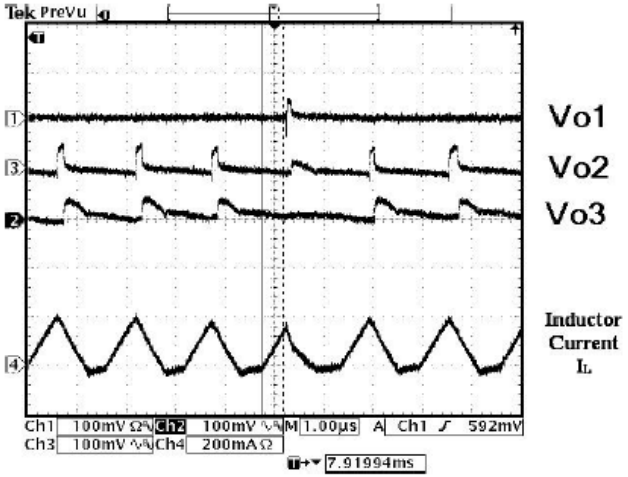


- 4 Positive boosted outputs + 1 dependent negative output

Measurement Results (1) – Normal operation

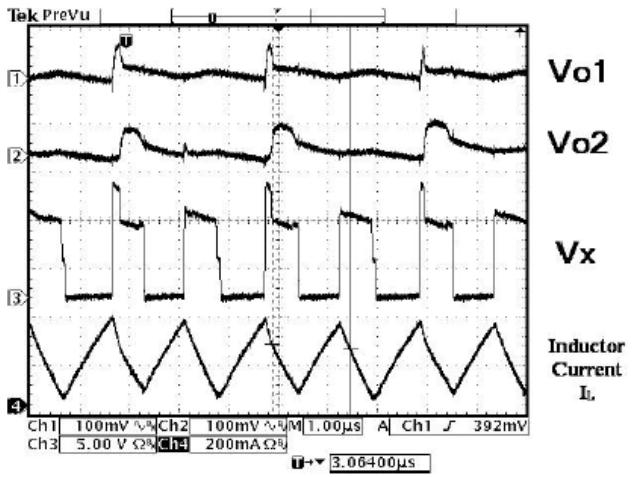
DCM

Vo1 = 10.2 V
Vo2 = 7.0 V
Vo3 = 7.5 V
Vo4 = 8.0 V

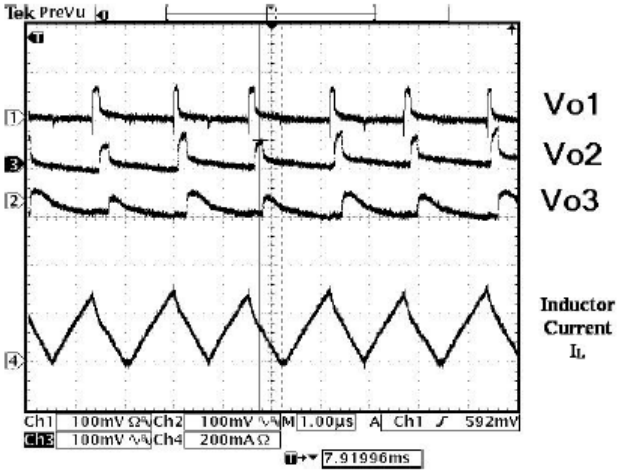


CCM

Vo1 = 10.2 V
Vo2 = 7.0 V
Vo3 = 7.5 V
Vo4 = 8.0 V

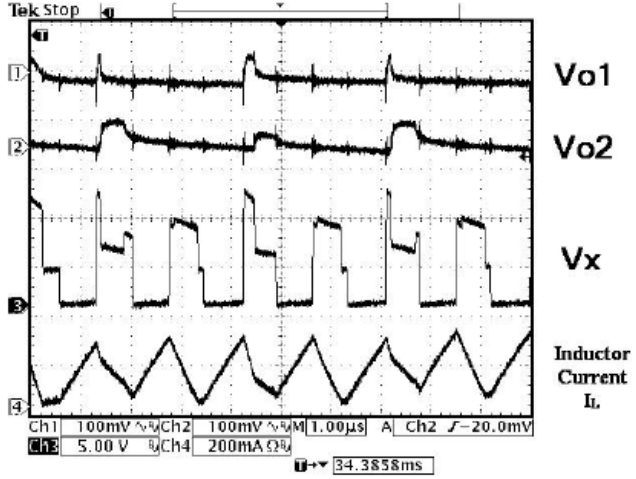


Vo1 = 10.2 V
Vo2 = 7.0 V
Vo3 = 7.5 V
Vo4 = 8.0 V



Boundary of DCM/CCM

Vo1 = 10.2 V
Vo2 = 5.0 V
Vo3 = 7.5 V
Vo4 = 8.0 V

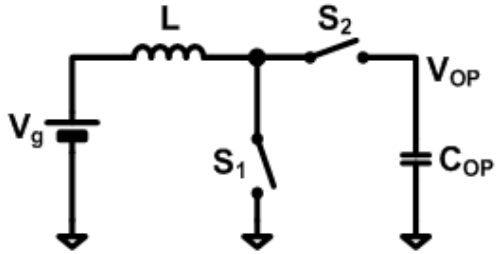


Boundary of DCM/CCM

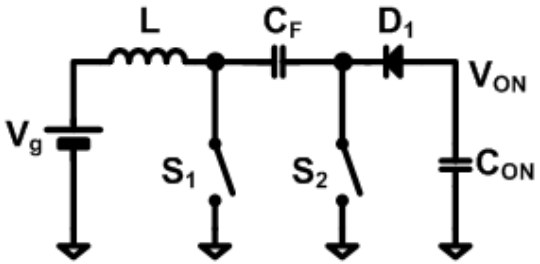
Performance Summary

Technology	0.5 μm Bi-CMOS, t-well, 3AL, 1PS				
Chip area	2.9 x 3.0 mm^2				
Package	QFN, 24 pins, 5 x 5 mm^2				
Supply voltage	2.5 ~ 4.5 V (3.7 V, nominal)				
Inductor/ESR	10 μH / 350 mΩ				
Oscillator frequency	700 KHz (nominal)				
Current ripple	290 mA				
Maximum efficiency	80.8 % @ 450 mW total load power				
Output	Vo1	Vo2	Vo3	Vo4	VoN
Voltage (V)	10.2	7.0	7.5	8.0	- 9.5
Load current (max) (mA)	5	30	30	40	5
Load regulation (mV/mA)	1.5	0.78	0.5	0.4	x
Line regulation (mV/V)	58	73	85	90	80
Output ripple (max) (mV)	160	140	140	120	200
Filtering capacitor/ESR (μF/mΩ)	4.7/300	4.7/300	4.7/300	4.7/300	1/150

2) Proposed SIBO converter



➢ Boost converter

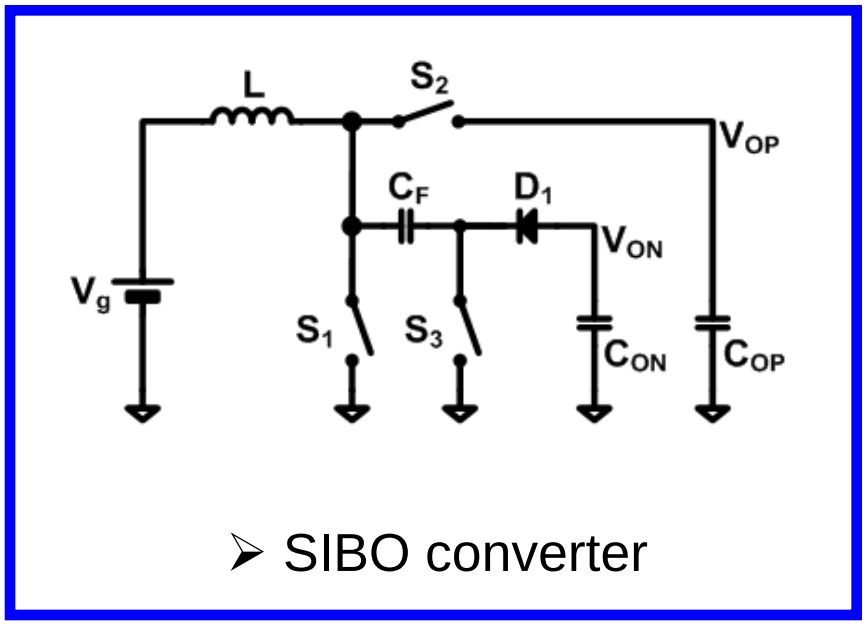


➢ Adjustable charge-pump

✓ 2 inductors, 4 switches

✓ Two PI-control

✓ Bulky & Expensive



➢ SIBO converter

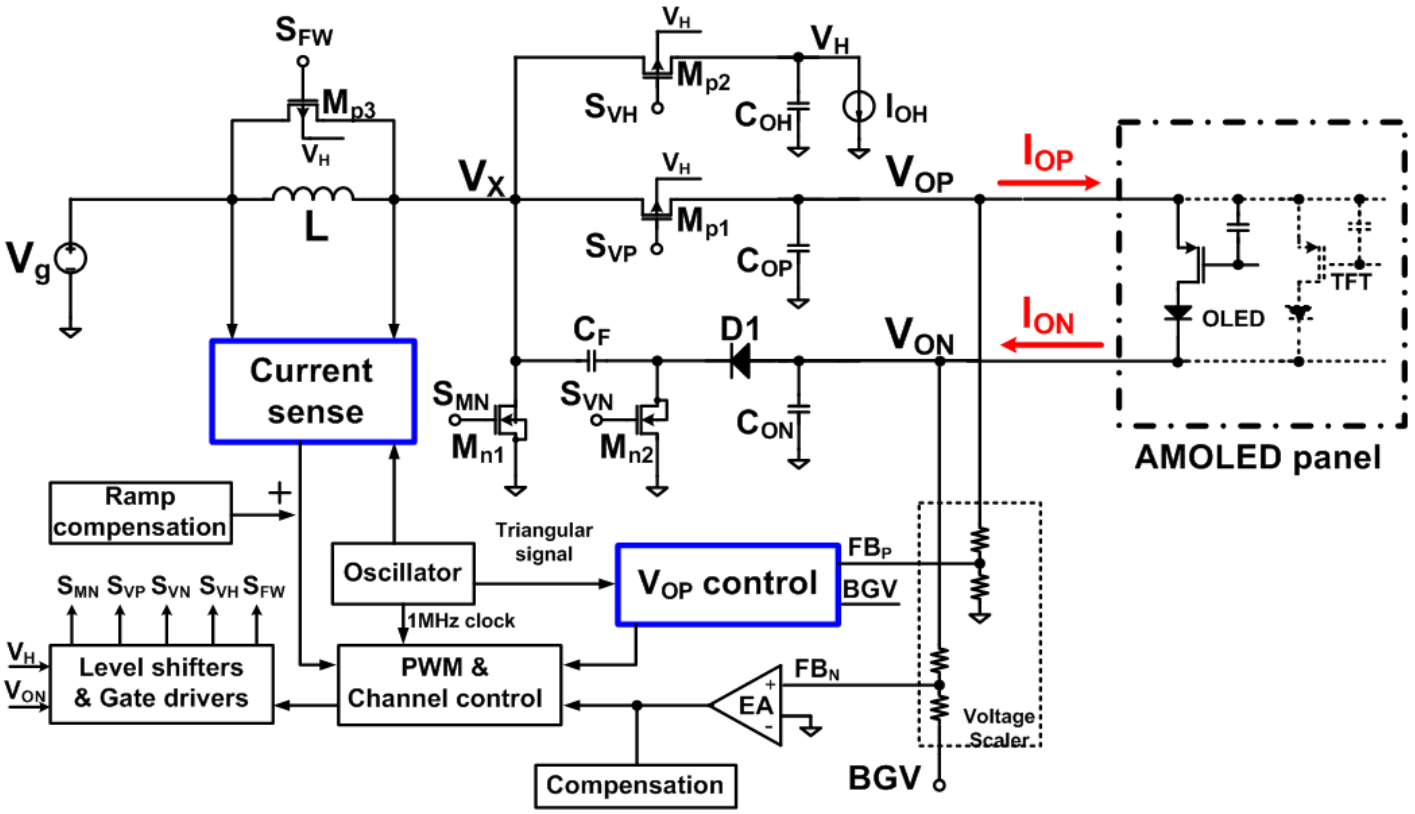
✓ 1 inductor, 3 switches

✓ Cost effective

✓ V_{OP} : Comparator control

✓ V_{ON} : PI-control

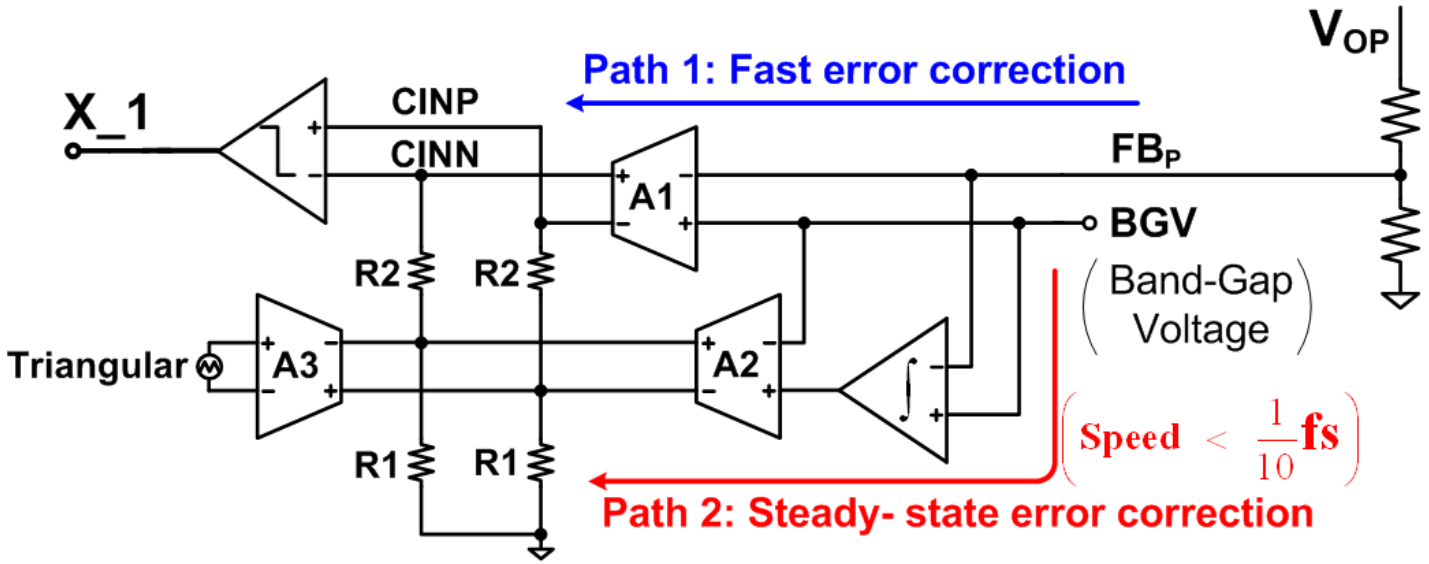
Implementation of SIBO converter

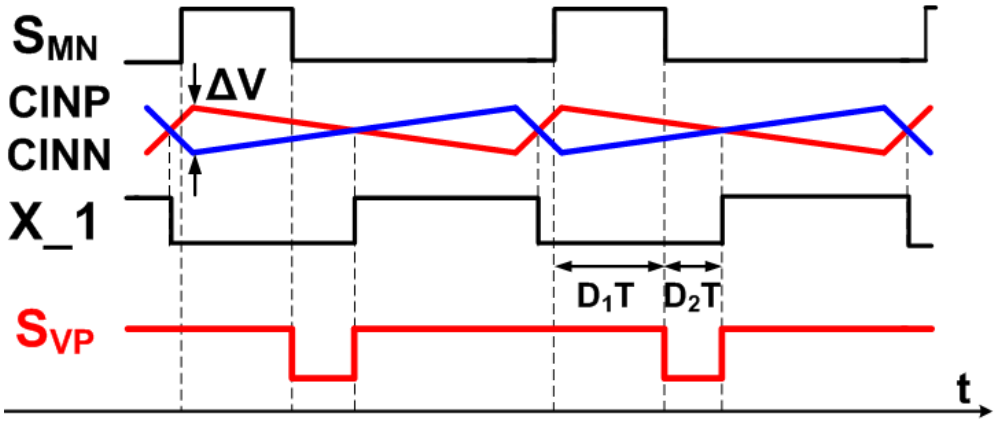


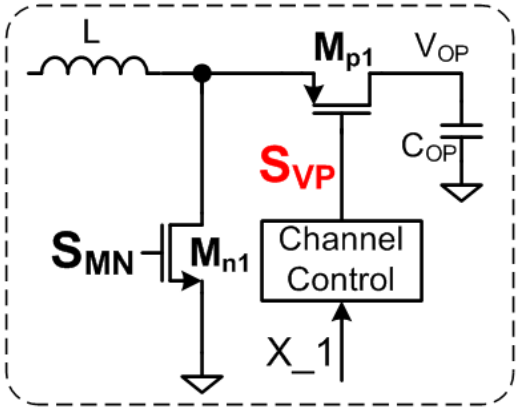
[Chae. ISSCC2007, JSSC 2009]

- Modified Comparator Control (MCC) based on OPDC

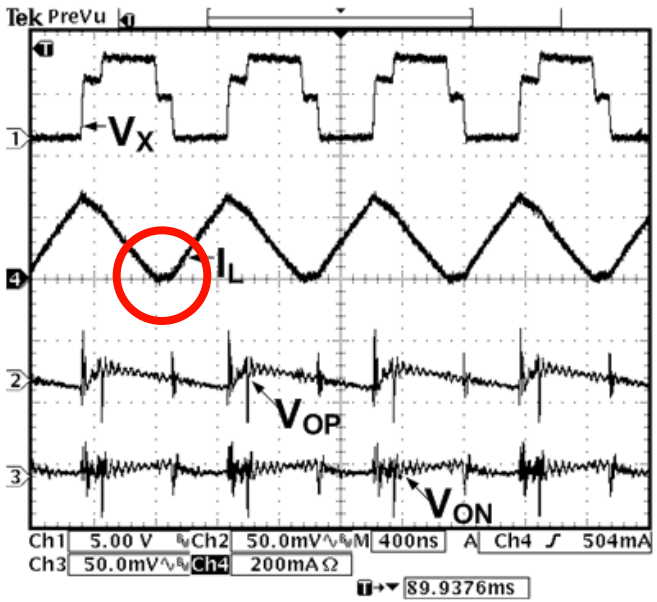
V_{OP} control (Modified Comparator Control)

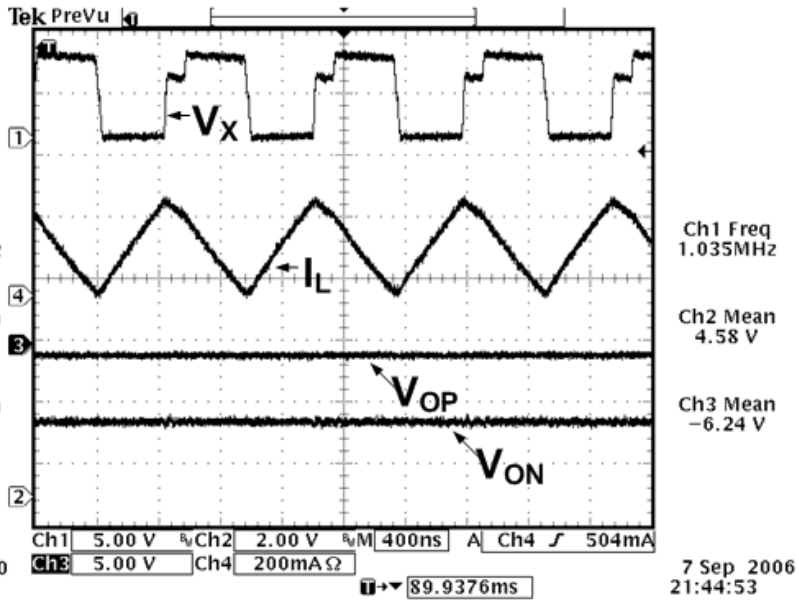






Measurement Results (1) – Normal operation





DCM operation

CCM operation

$I_{OP}=I_{ON}$=20mA @ Vg=3.7V

Freewheel switching

$I_{OP}=I_{ON}$=35mA @ Vg=3.7V

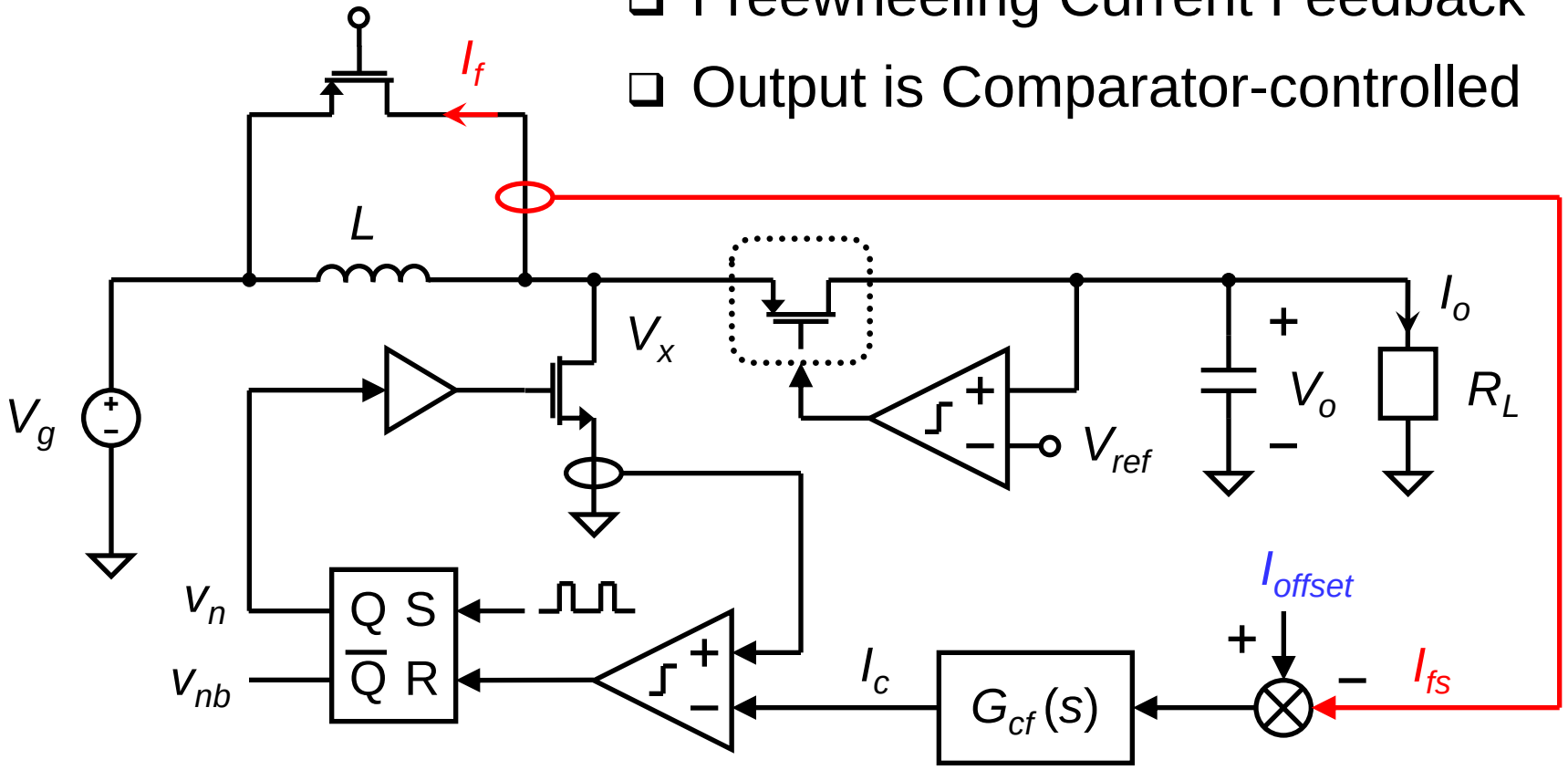
No Freewheel switching

Performance Summary

Process	0.5μm Power BiCMOS	
Chip area	4.1mm^2	
Battery voltage range	2.7~4.5V (3.7V, nominal)	
Inductor / ESR	4.7μH / 320mΩ	
Oscillator frequency	1MHz (nominal)	
Maximum efficiency	82.3%	
Current ripple ΔI	240mA	
Output voltages	V_{OP} (4.58V)	V_{ON} (-6.24V)
Output ripples	15mV	5mV
Load regulation	0.25mV/mA	1mV/mA
Line regulation	6mV/V	18mV/V
Filtering capacitors / ESR	4.7μF / 20mΩ	4.7μF / 20mΩ

3) Freewheeling Current Regulation

- Freewheeling Current Feedback
- Output is Comparator-controlled

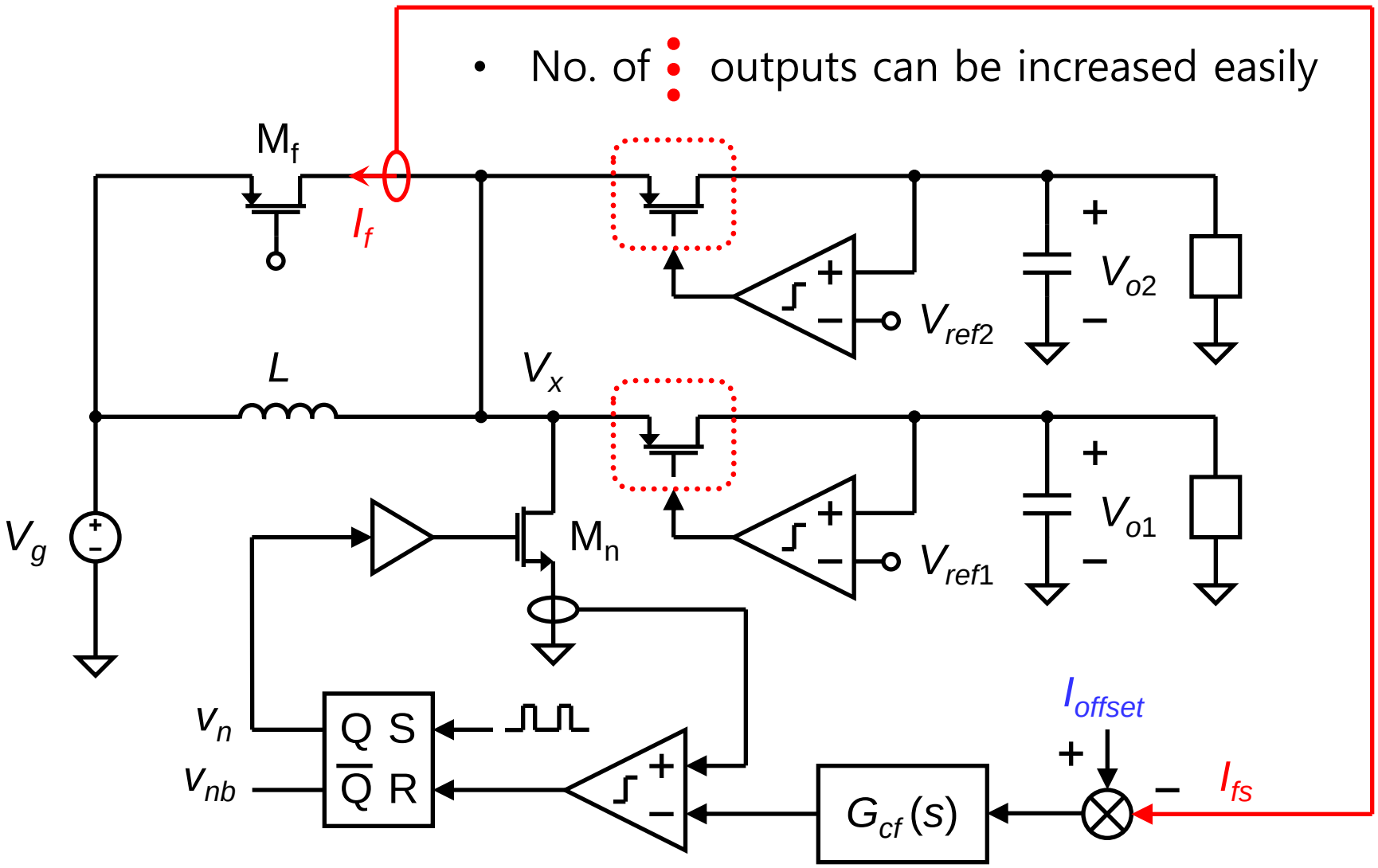


- Output Cap. and Load Current do NOT affect the Loop
- Compensator Design is EASY

Pros and Cons

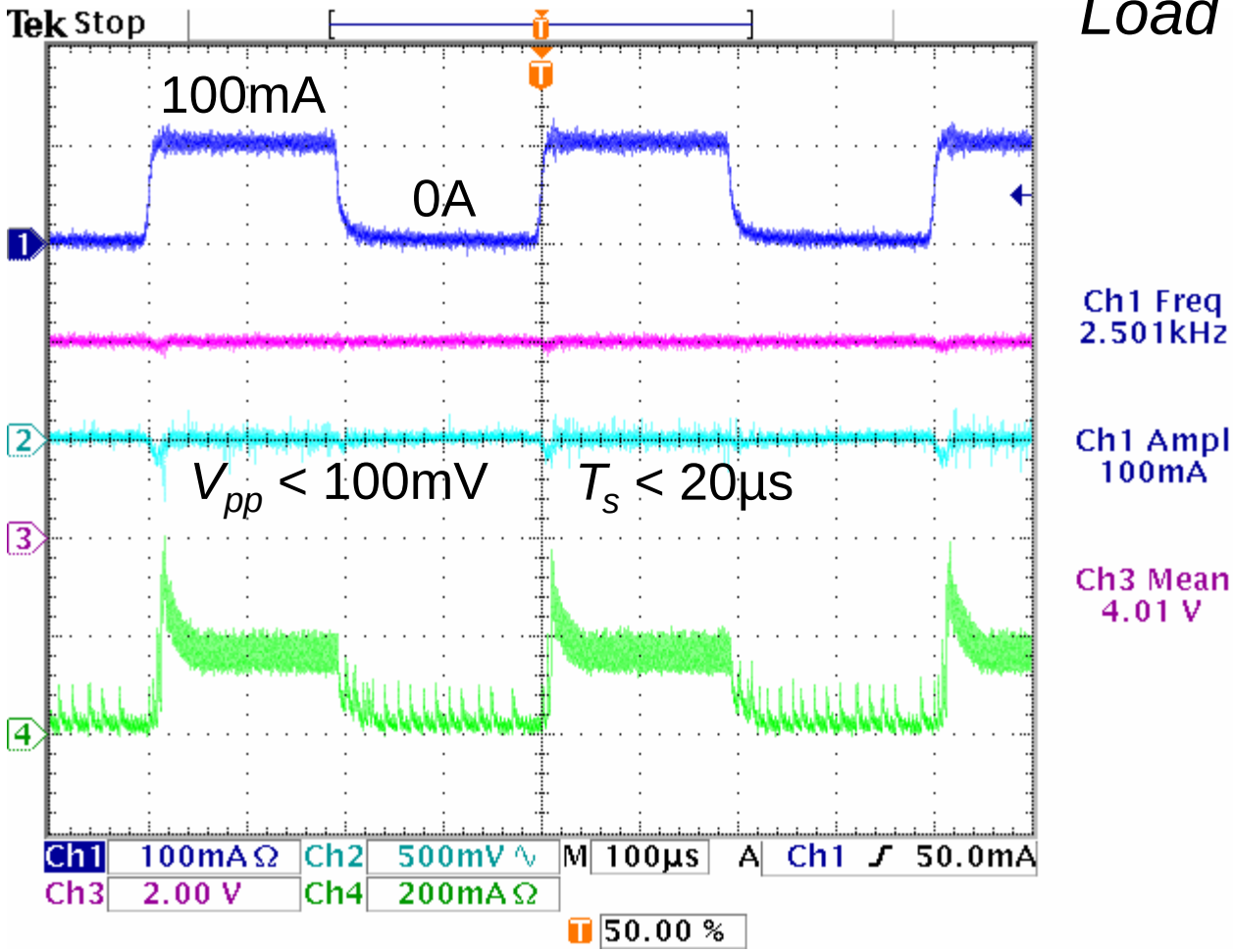
Control Scheme	Loop Dynamics	Main Features
Direct Duty Control w/ Output Voltage Feedback	L, C_o	**- Complex Compensation** **- Slow Response**
***Current Mode Control* w/ Output Voltage Feedback**	L, C_o	**- Difficulty in Compensation for a Wide Load Range**
Current Mode Control* w/ *Freewheeling Current Feedback	L, C_o	**+ Load Independent** **+ Simple Wide-Bandwidth Control** **- Power Switch for Freewheeling** **- Small Decrease in Efficiency**

Control of Multiple Output Converter



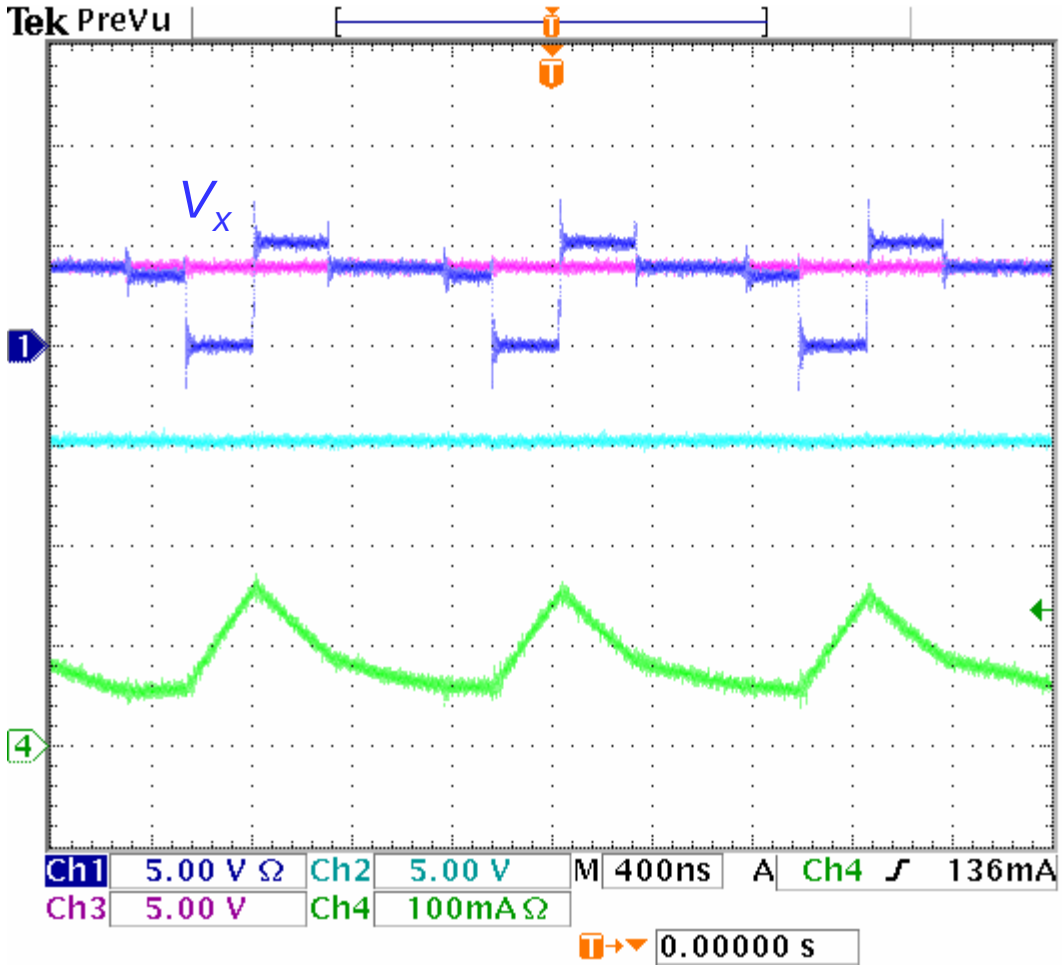
Measured Waveforms

Load Transient



Measured Waveforms

Steady State



$I_{op} = I_{on} = 23\text{mA}$

Measured Performance

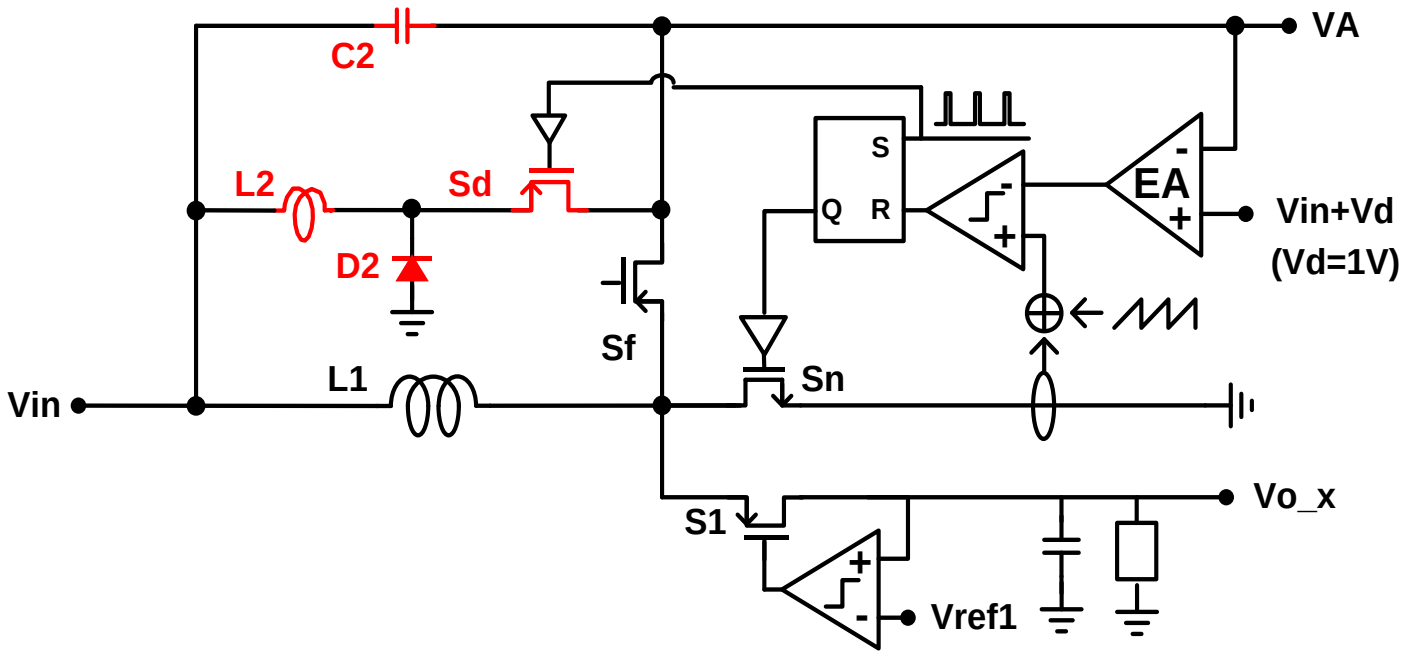
Technology	**0.5μm Power BiCMOS**
Area	**3.2mm^2**
Supply Voltage	**3.7V nominal (2.7 ~ 4.5V)**
Inductor / ESR	**10μH / 350mΩ**
Switching Frequency	**1MHz**
Filtering Capacitor	**10μF Tantal // 470nF Ceramic**
Maximum Efficiency	**81% ***
Load Transient (No Load to 100mA)	**$V_{o,pp}$ < 100mV, T_s < 20μs ****

* 82.3% achieved in [Chae, ISSCC07].

** These values do not represent the best achievable results.

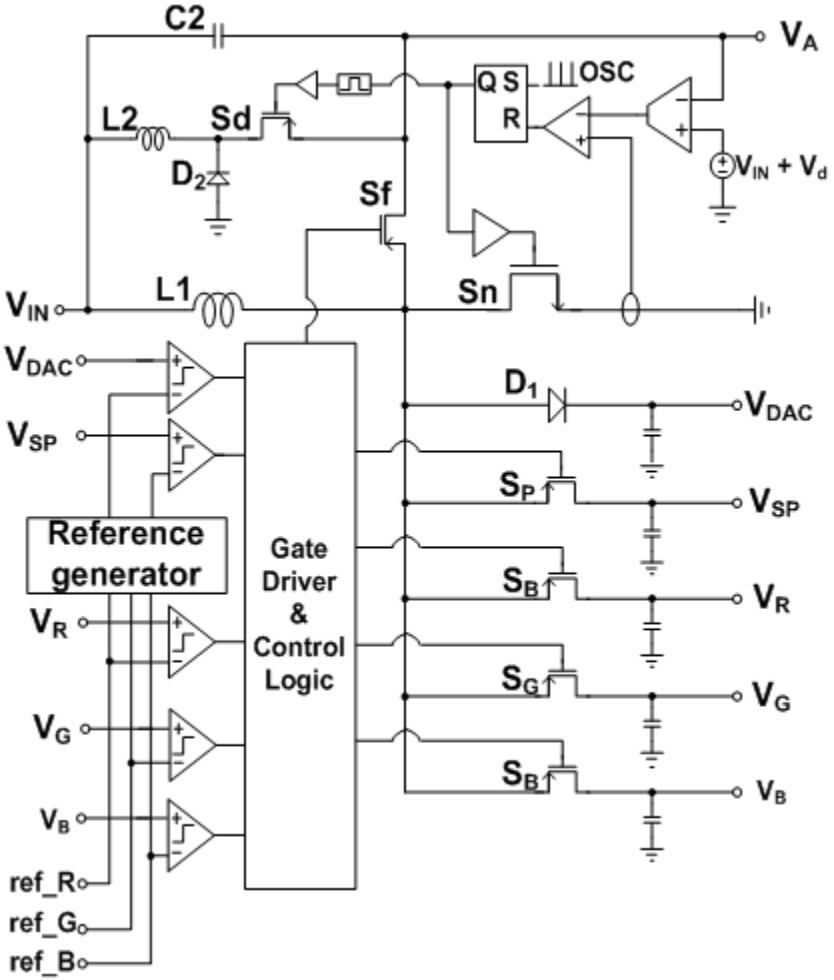
4) Vestigial Current Regulation

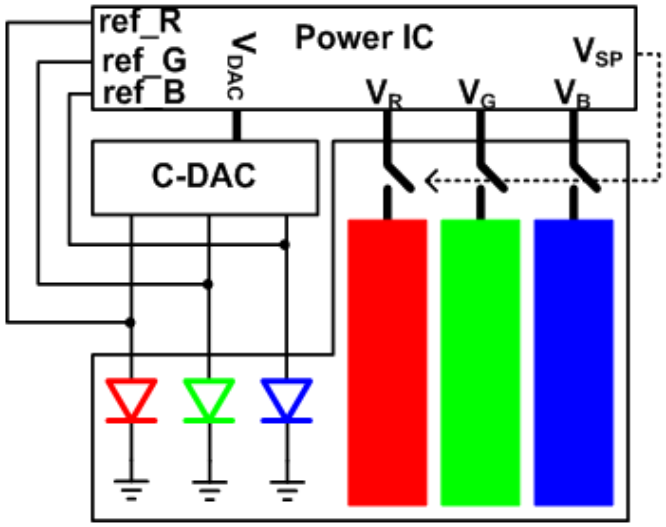
(Seol, ISSCC09)



- Auxiliary Output VA Feedback
- Output Cap. and I_O affect the Loop Response(LIC)
- Additional components are Needed

Implementation of Multiple Output Converter

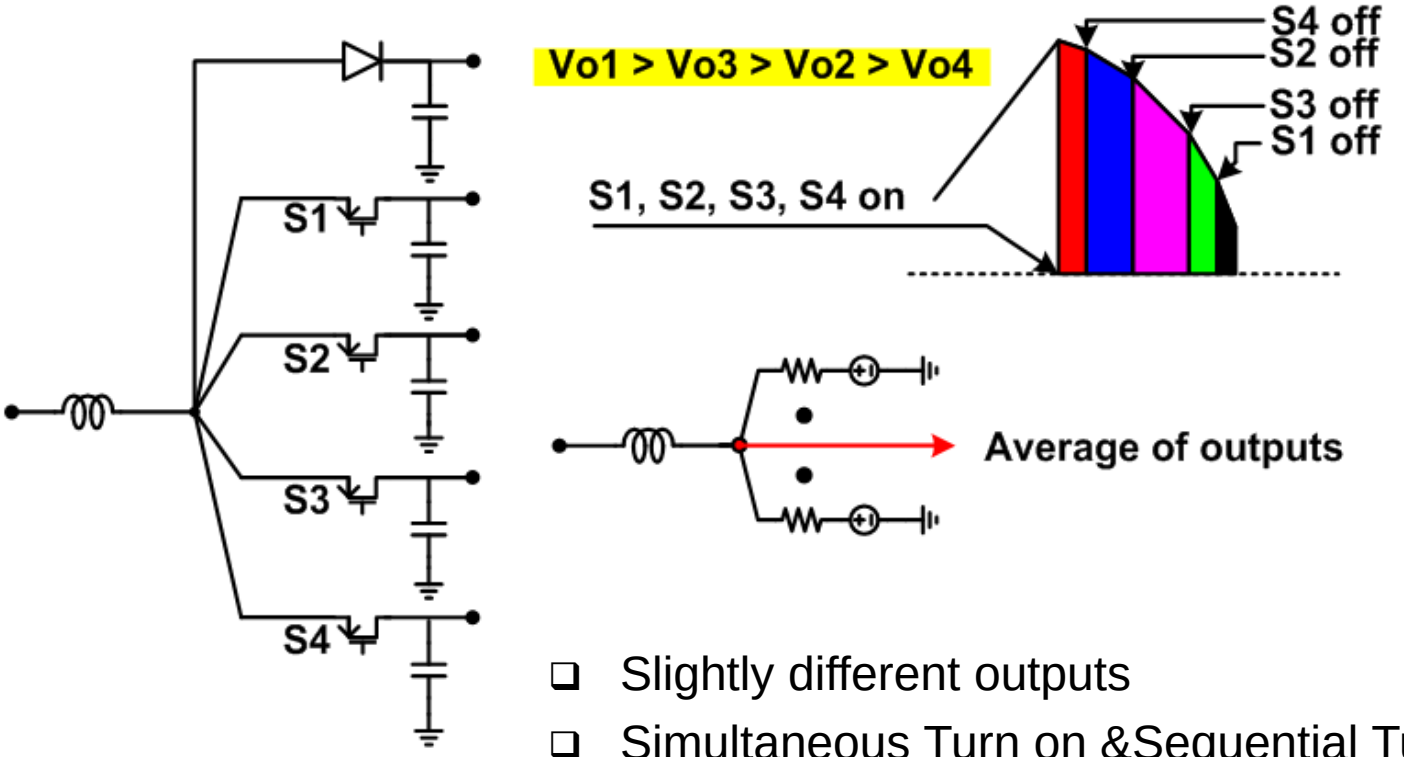




- Vin: 2.8 ~ 4.5 V
- $V_{R,G,B}$: 2 ~ 9 V
- V_{SP}: Higher than $V_{R,G,B}$ by 0.5 V (Lower limit 6.3V)

❑ V_{DAC}: Higher than V_{SP} by 2V (Lower limit 8.3V)

Output switching control

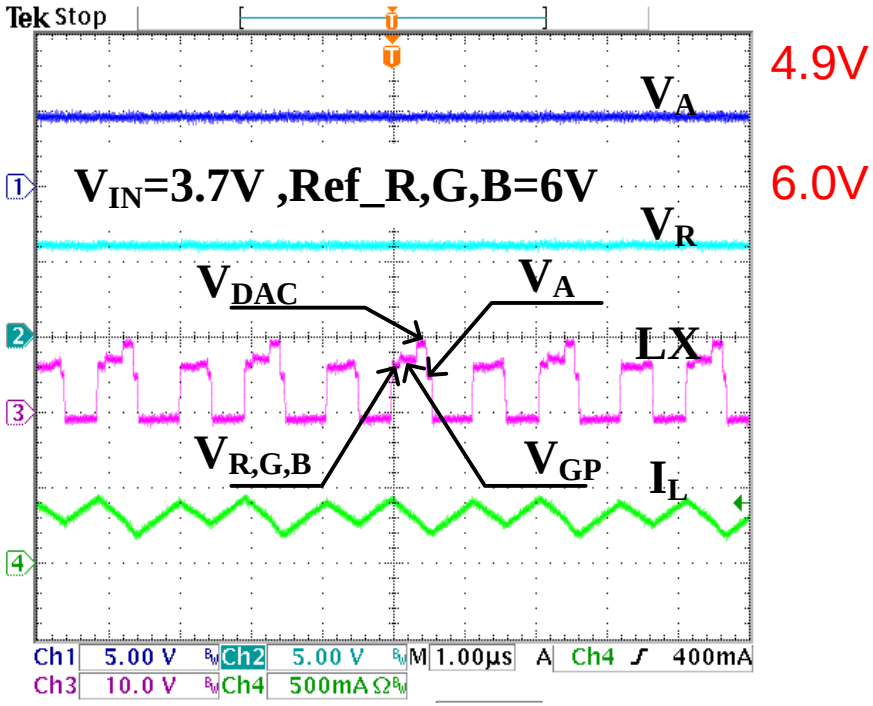


- Slightly different outputs
- Simultaneous Turn on &Sequential Turn off

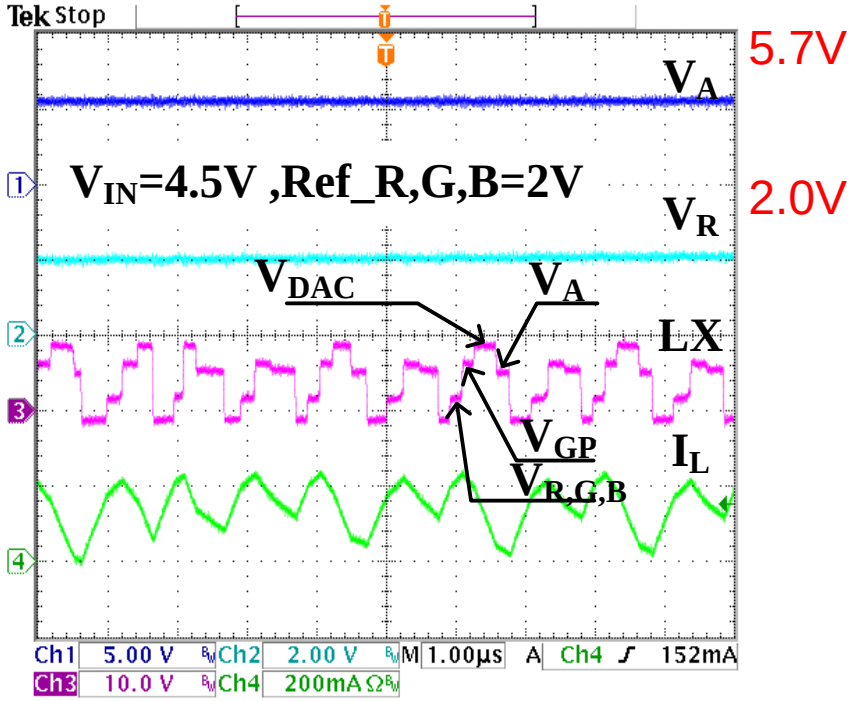
- Averaging of outputs by simultaneous switching
- Discharging of inductor current by the averaged voltage
- Enforced averaging effect by the charging sharing between outputs
- Chaotic switching is alleviated by the averaging effect

Measurements Results

- Normal operating waveforms



<Step up>



<Step down>

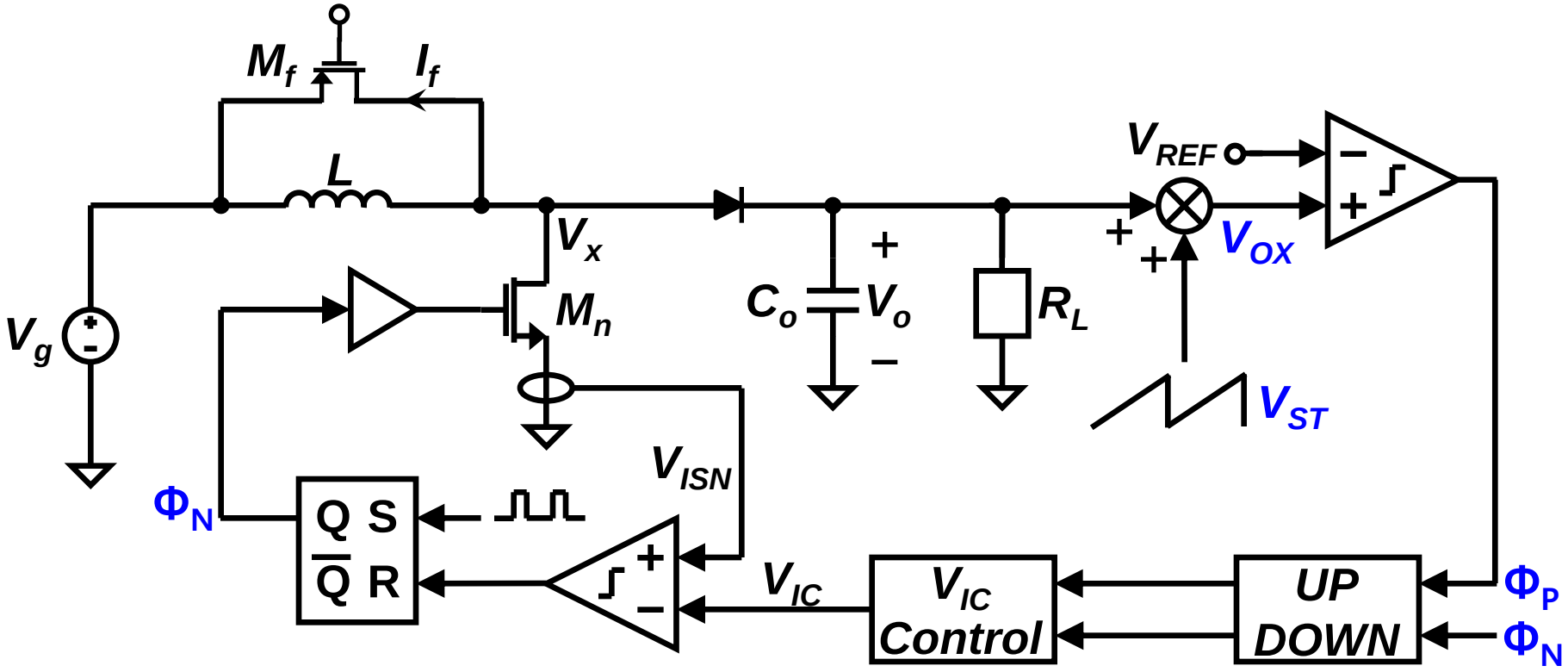
Performance Summary

Process	0.5μm 1P3M BiCMOS
f_{SW}	1MHz
V_{DAC}	8 ~ 12V, 20mA
V_{GP}	6 ~ 10V, 30mA
$V_{R,G,B}$	2 ~ 9.5V, 25, 25, 45mA
Accuracy	0.1 % [1.5%]*
Line regulation	0.05 %/V** [1.04%/V]
Load regulation	0.01 %/mA*** [0.015%/mA]
Efficiency	83 % **** [80%]

*[] result of [2] **V_{IN}= 2.5 to 4.5 V ***0mA to $I_{\_load}$ @V_{IN}= 3.7 V

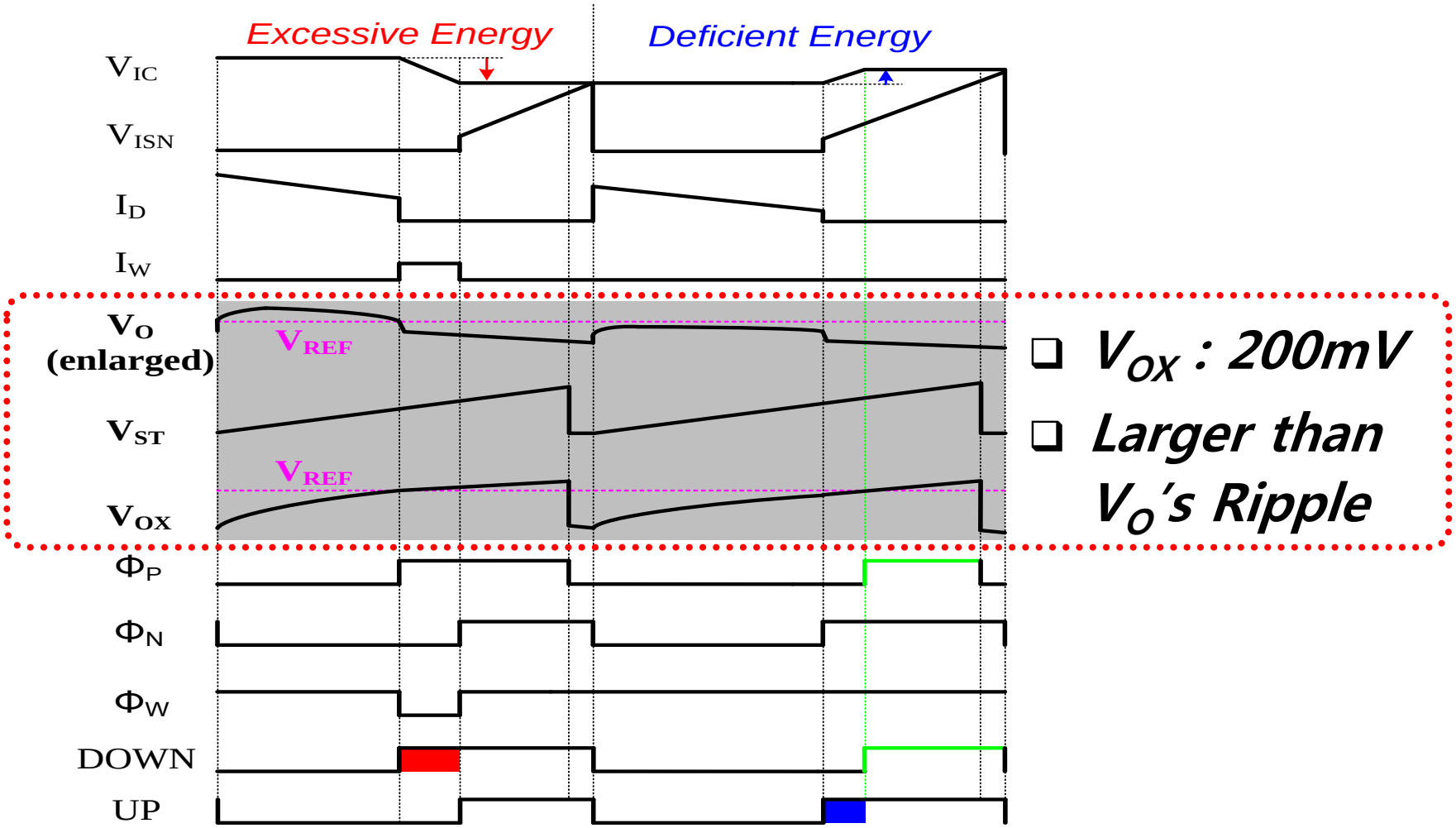
****@ V_{IN}= 3.7 V, Ref=6, $I_{\_load}$=25$_{_R}$, 25$_{_G}$, 45$_{_B}$,30$_{_GP}$,10$_{_DAC}$

5) Proposed Zero-Order Control



- Loop response is independent of *L* & *Co*
- I_f is Zero in steady-state : No decreasing Power Efficiency
- Control Loop is Simple

The Role of V_{ST}

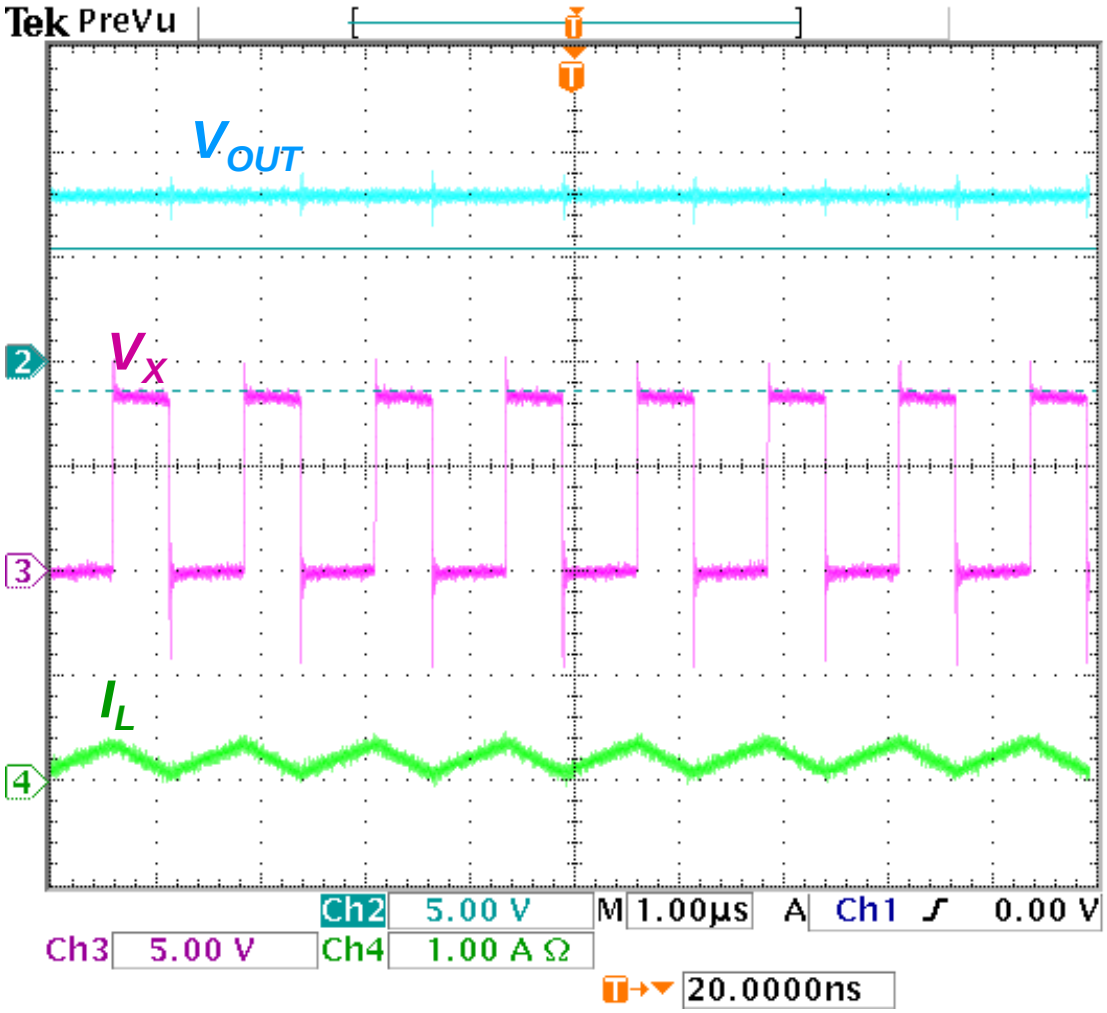


- *Make Φ_P go to High even when deficient energy case*
- *V_{ST} causes small Offset Voltage – corrected by MCC*

Pros(+) and Cons(-) - ZOC

Control Scheme	Loop Dynamics	Main Features
FW Current Control	~~L, C_o~~	- Extra Energy - Power Switch for Freewheeling - Decrease in Efficiency
Auxiliary *Output Voltage Control*	~~L, C_o~~	+ Vestigial Current is returned - Extra Energy - Additional Components for VA
Zero-Order Control	~~L, C_o~~	+ Balanced Energy + No Decrease in Efficiency + No Additional Components

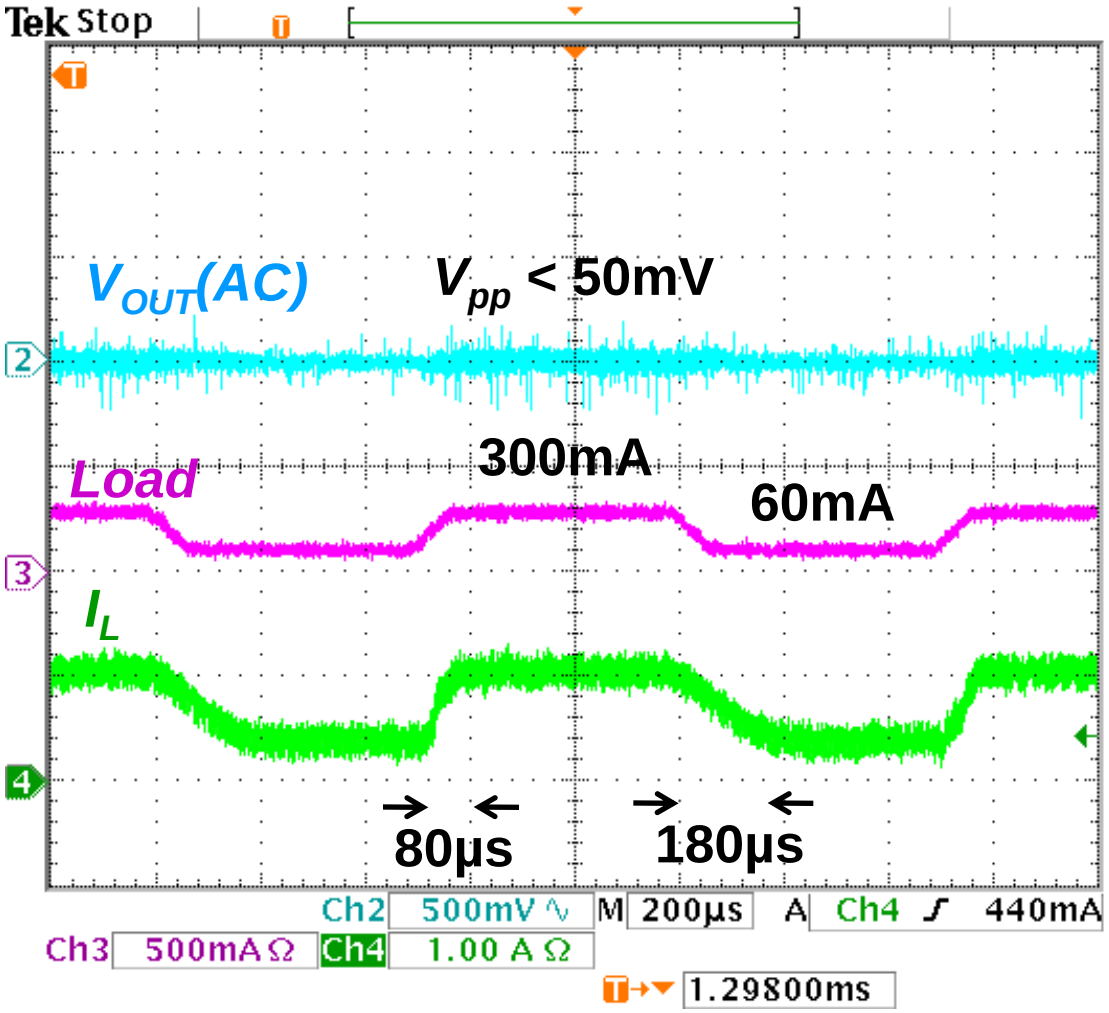
Measured Waveforms



Steady State - CCM

- ***Load = 60mA***
- ***No FW period***

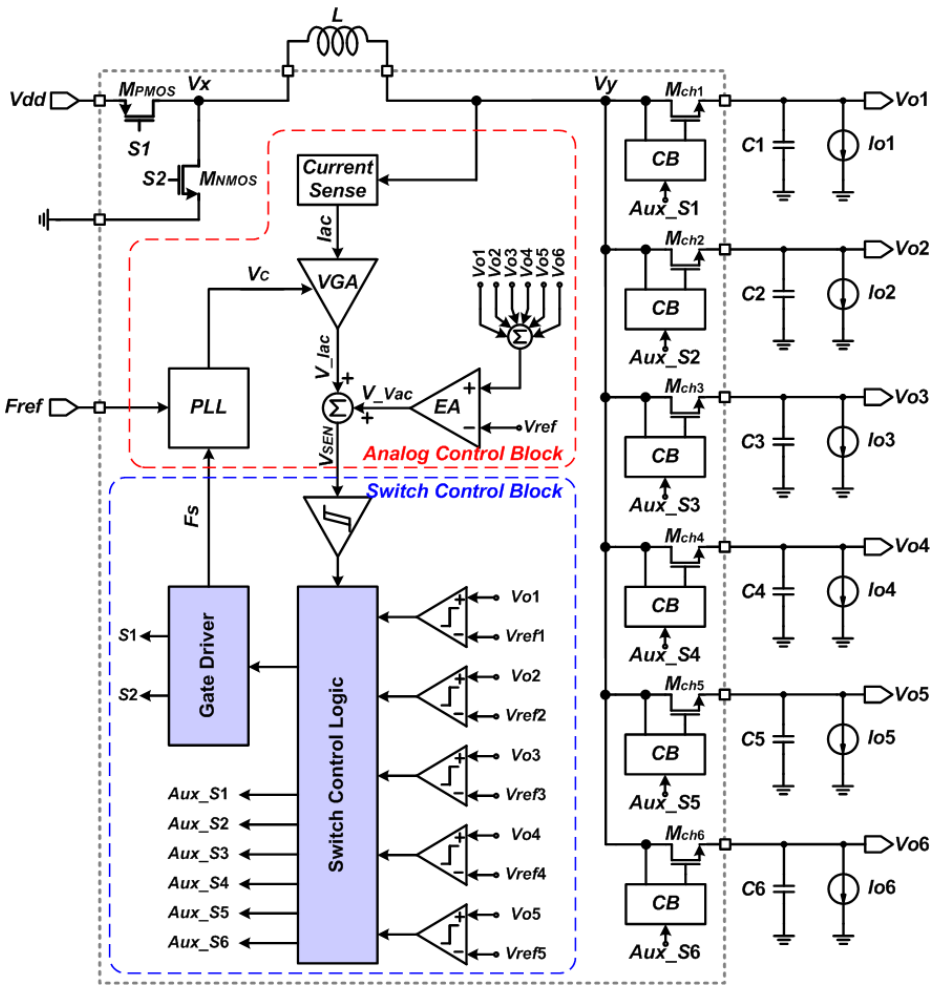
Measured Waveforms



Load Transient

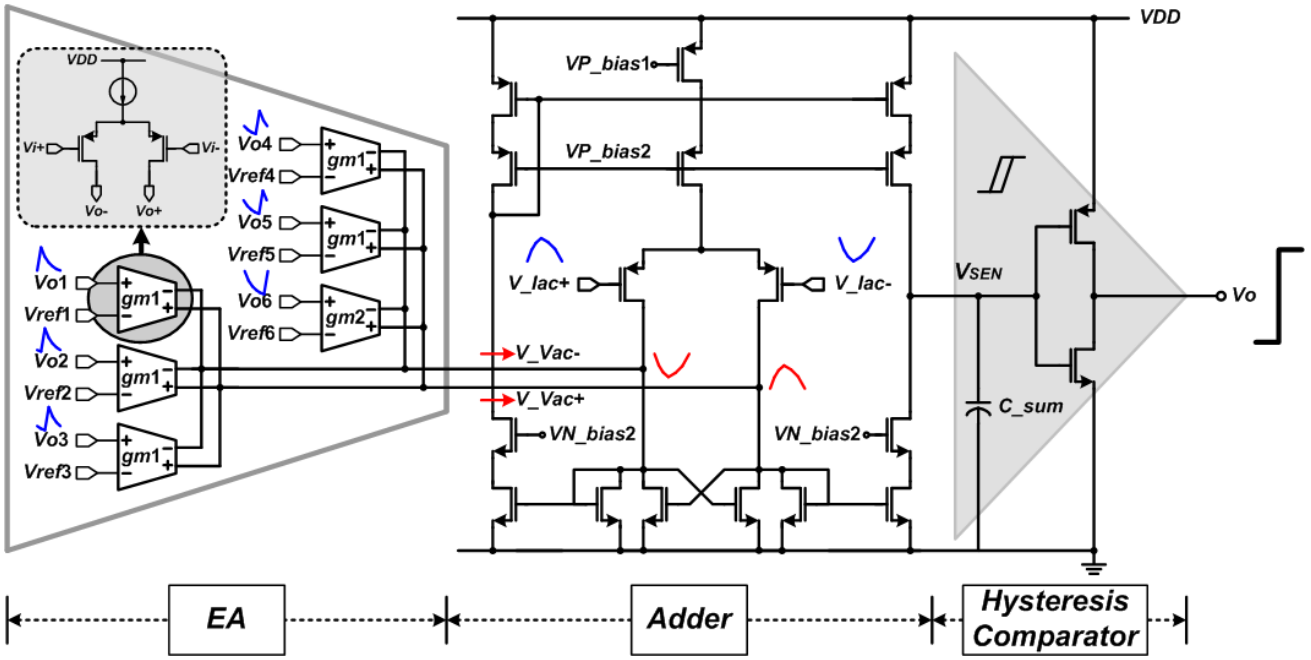
6) PLL based SIMO buck converter

- ✓ Switching frequency
  - Constant
  - High
- ✓ Switch control
  - Comparator control
  - PMB control
- ✓ Bang-bang control
  - Stable
  - Fast and accurate regulation



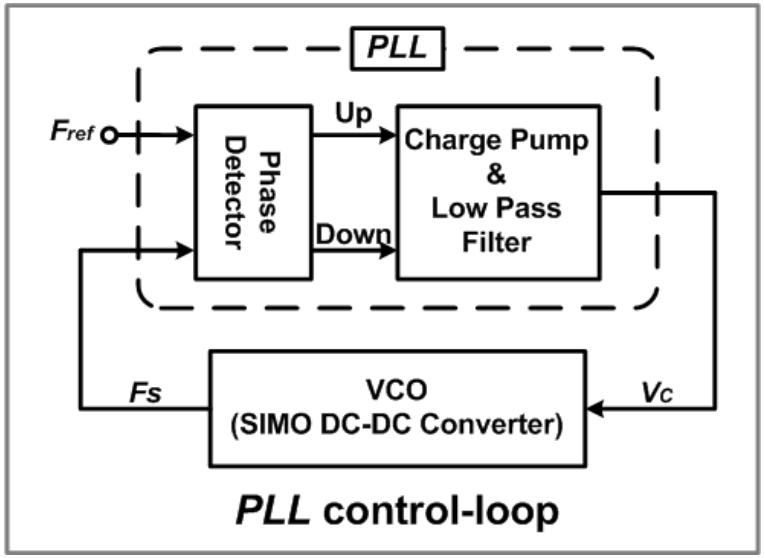
PMB Control (Vo6)

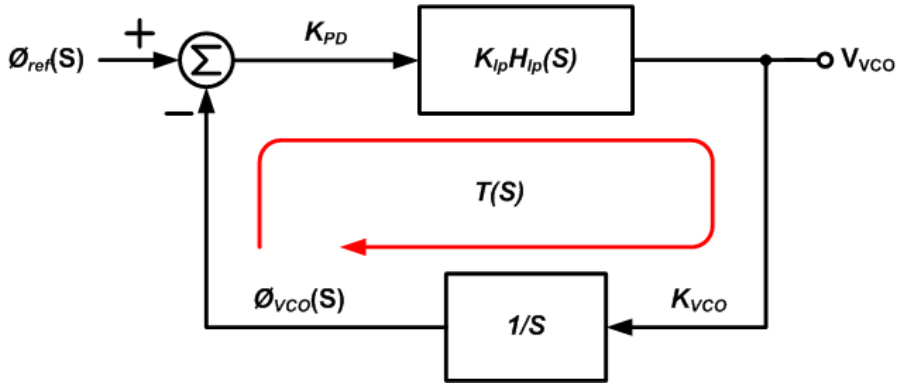
PMB : *PLL-based Multiple-Output Bang-Bang*

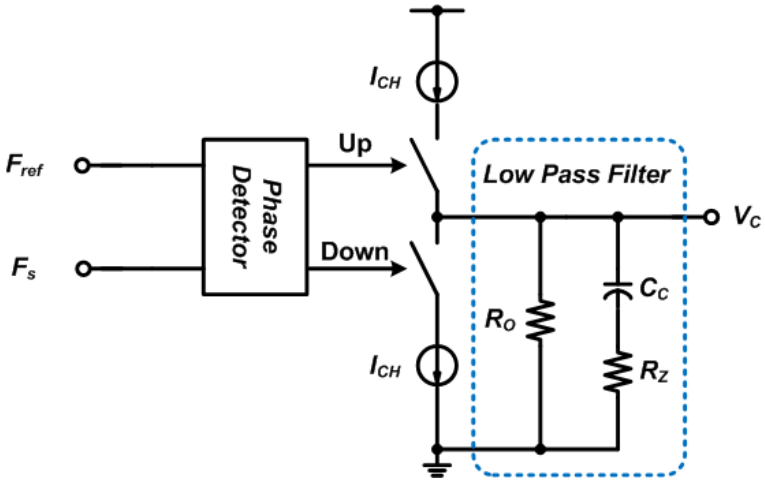


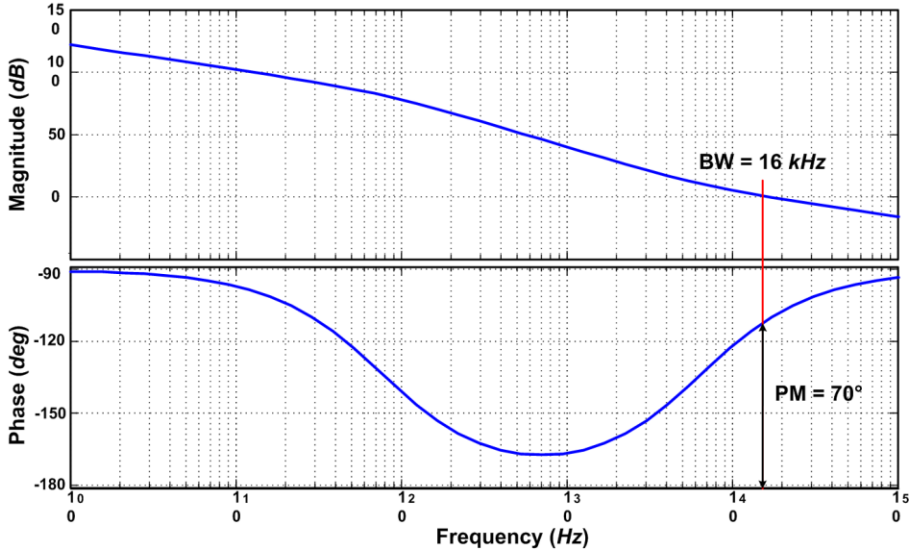
- ☑ In-Phase Voltage information of error voltage is reproduced by error amplifier (*EA*).
- ☑ *Hysteresis comparator* is implemented by the inverter and capacitor through the system delay.

Loop Analysis of the switching converter

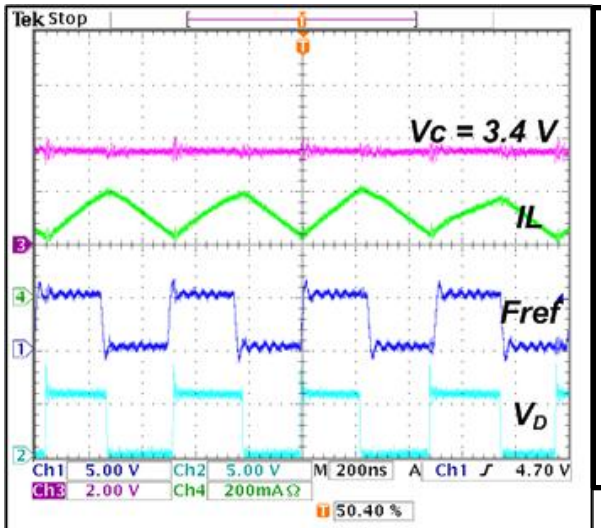


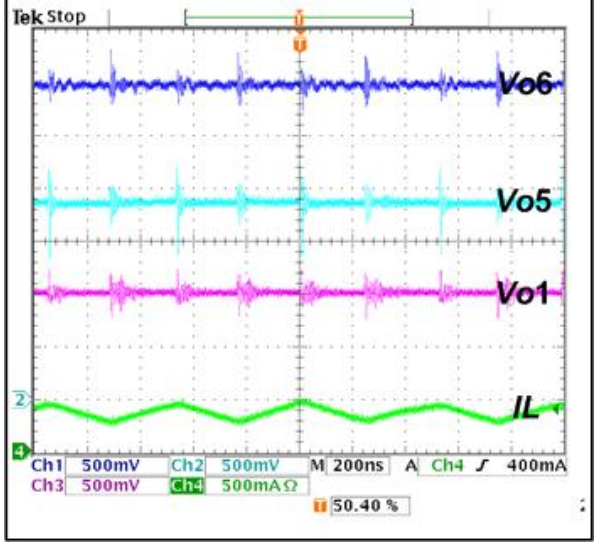




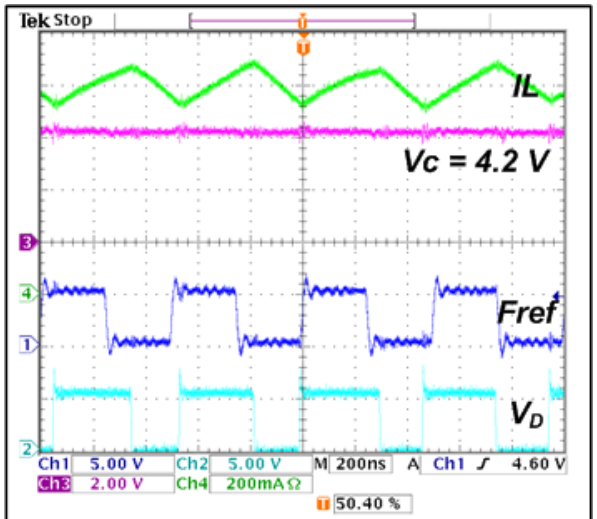


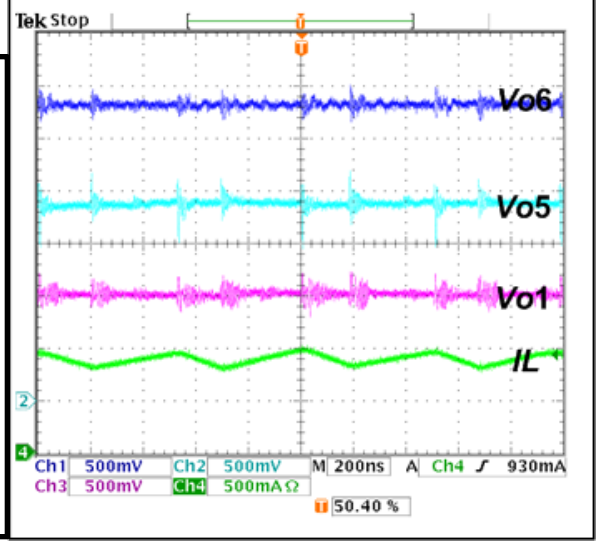
Waveform at the Steady State





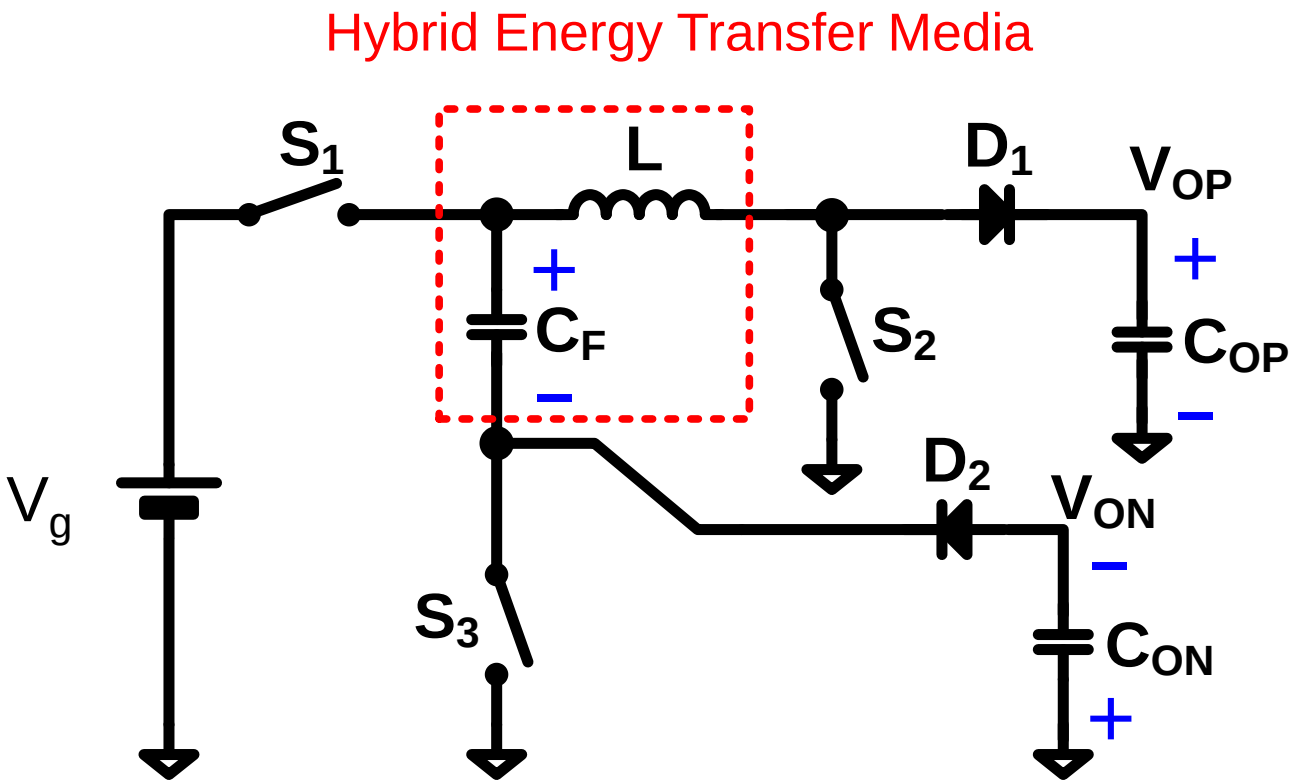
Io1 = 22mA,
Io2 = 28mA,
Io3 = 32mA,
Io4 = 20mA,
Io5 = 19mA,
Io6 = 30mA.





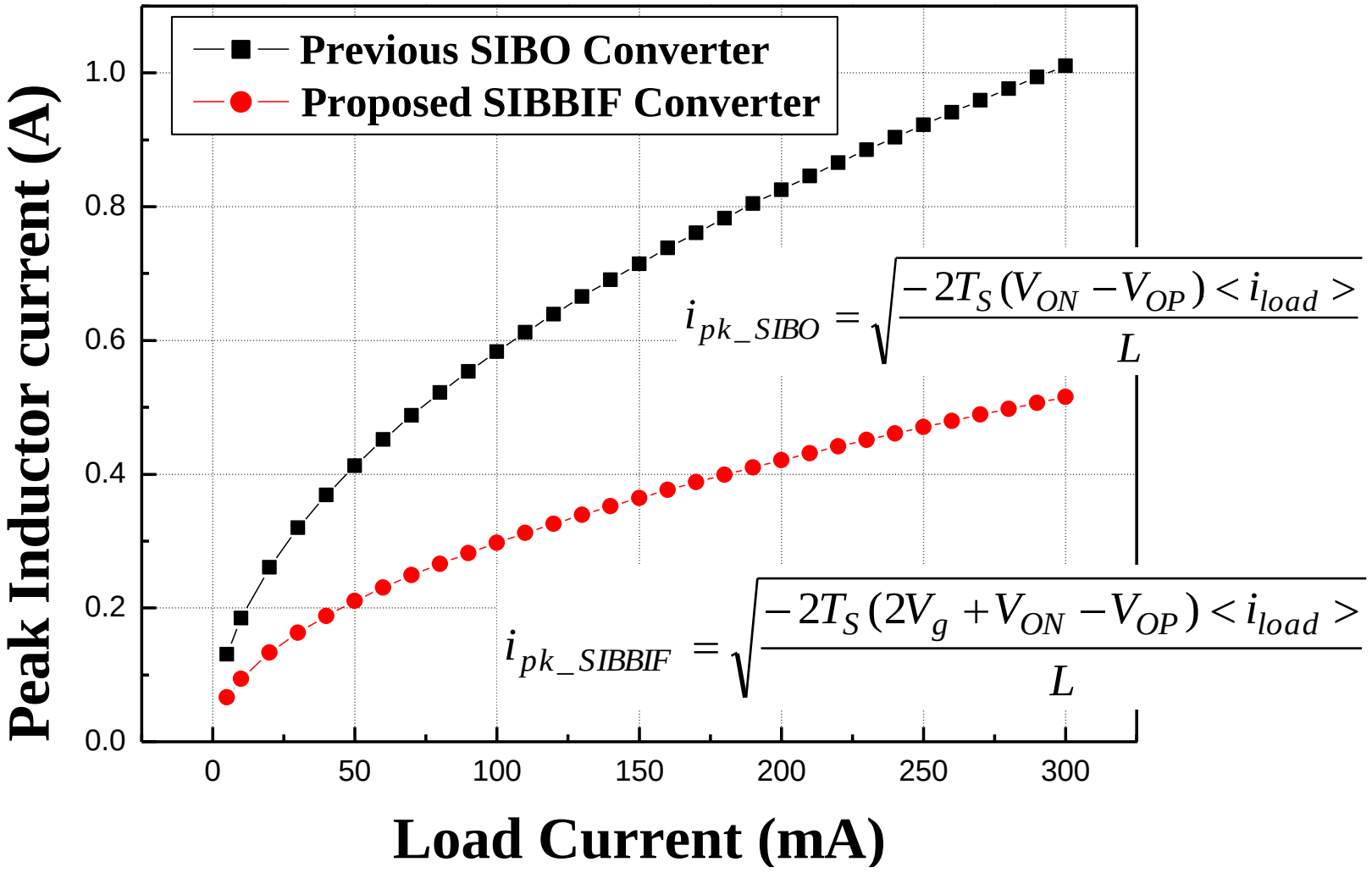
Io1 = 100mA, Io2 = 130mA, Io3 = 100mA, Io4 = 130mA, Io5 = 127mA.

7) Proposed SIBBIF Converter (Architecture)

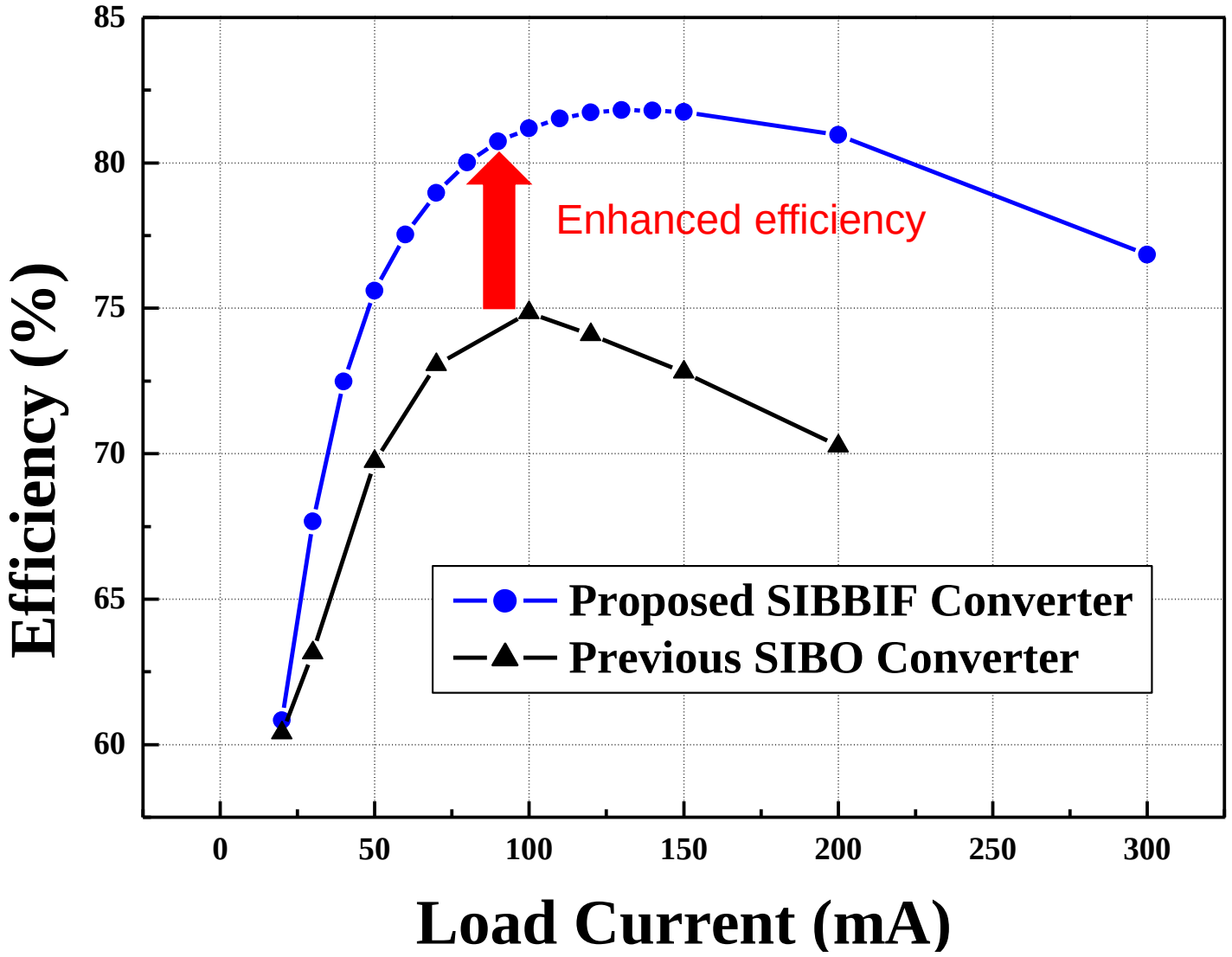


- Vg : Li-ion battery(2.7V ~ 4.5V), USB(5V)
- V_{OP} : 4.6V by boost or buck operation
- V_{ON} : -5.4V by inverting flyback operation

Calculated peak current comparison

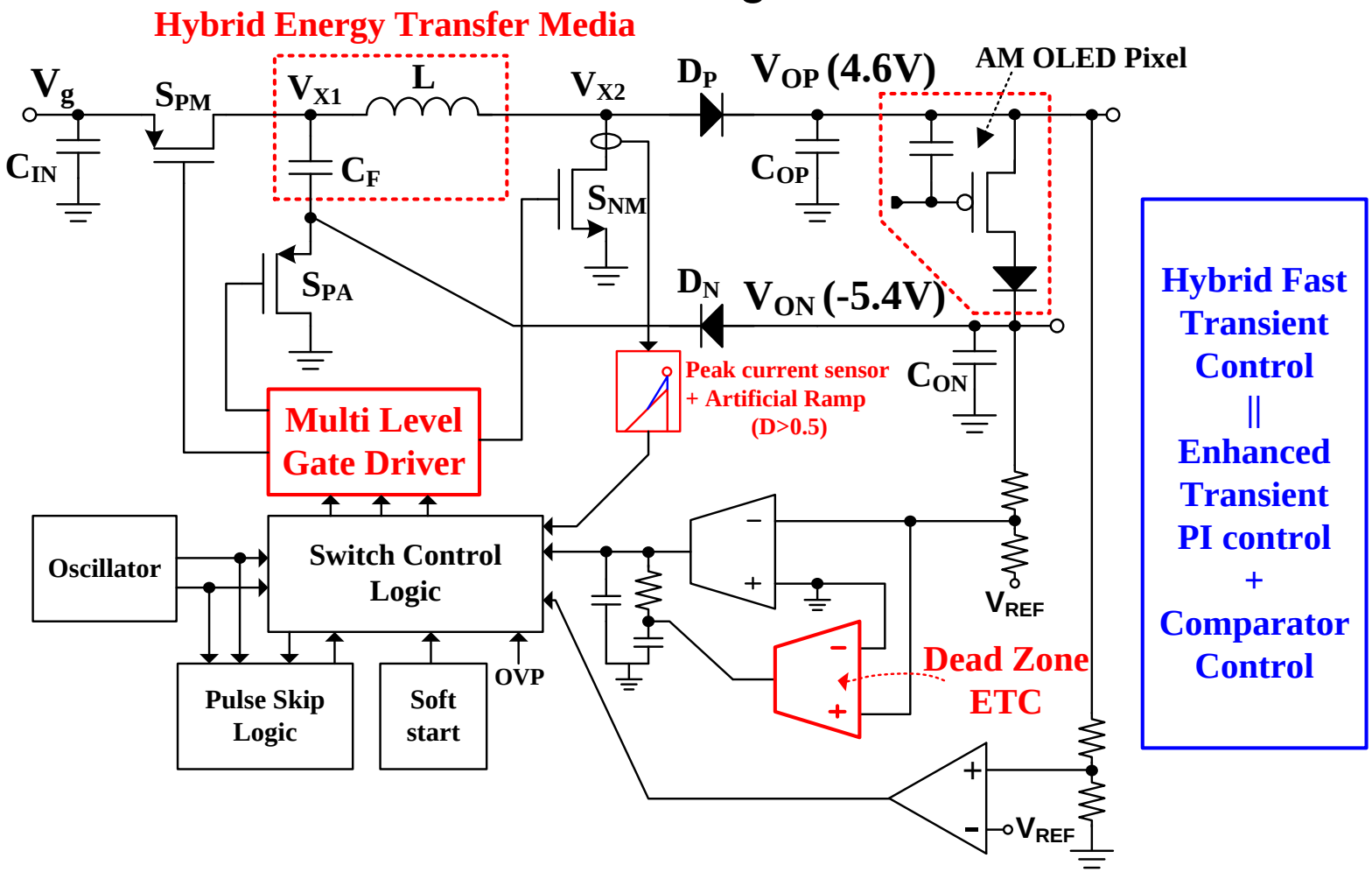


Simulated efficiency comparison

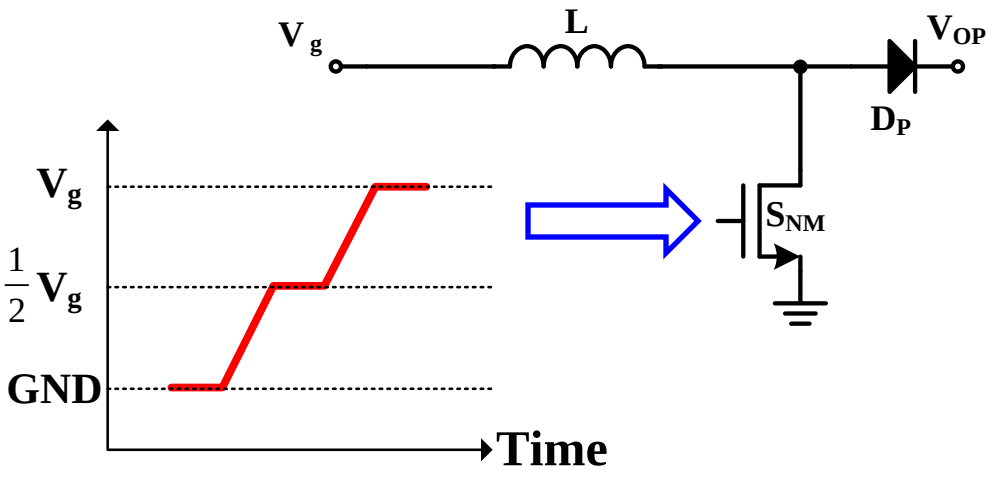


Proposed SIBBIF Converter

Block Diagram



Multi Level Gate Driver



Conventional Gate Driving

$$(1) P_{SW} = C_g \times V_g{}^2 \times F_S$$

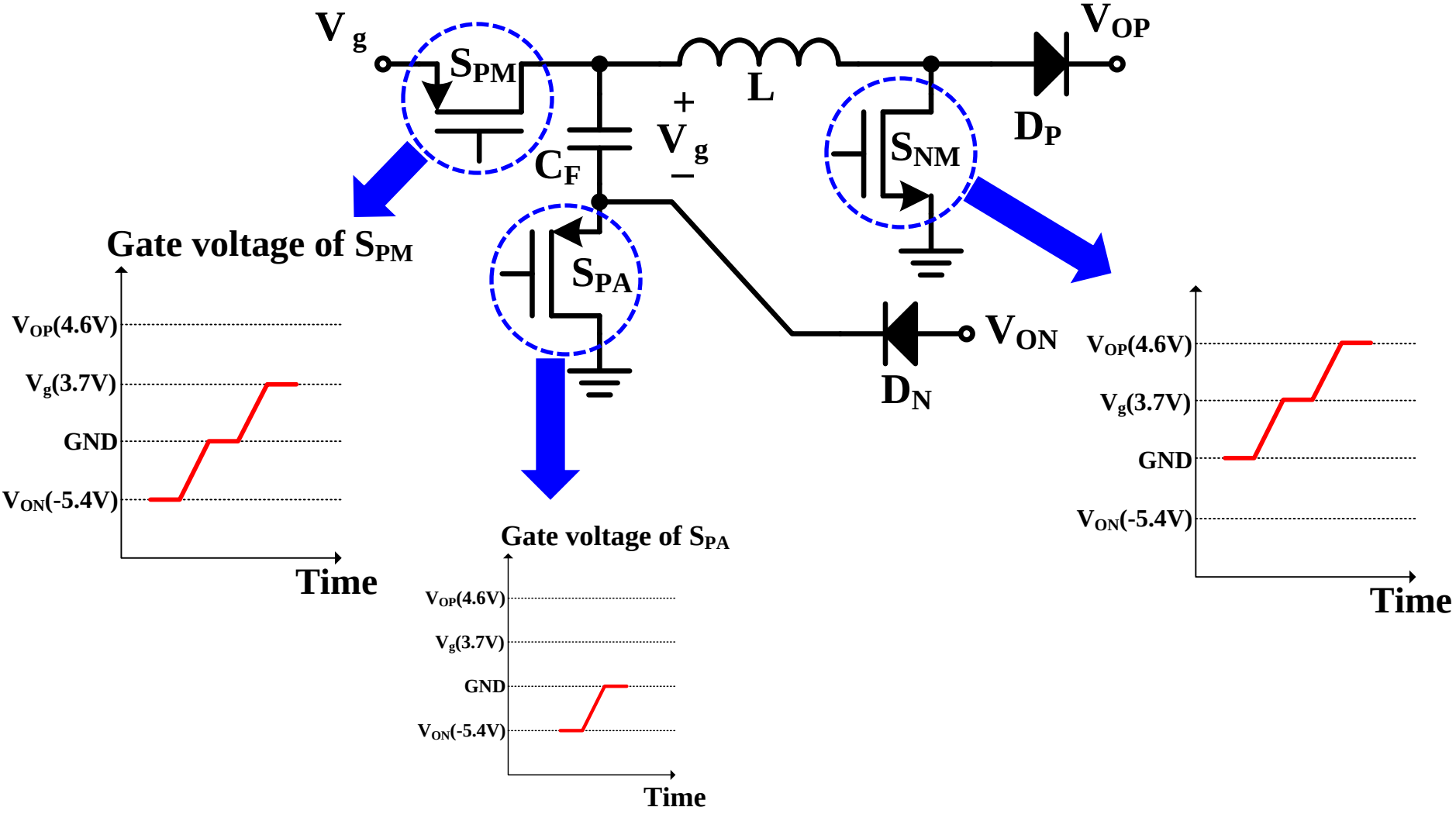
Multi Level Gate Driving

$$(2) P_{SW} = C_g \times (\frac{1}{2} V_g)^2 \times 2F_S$$

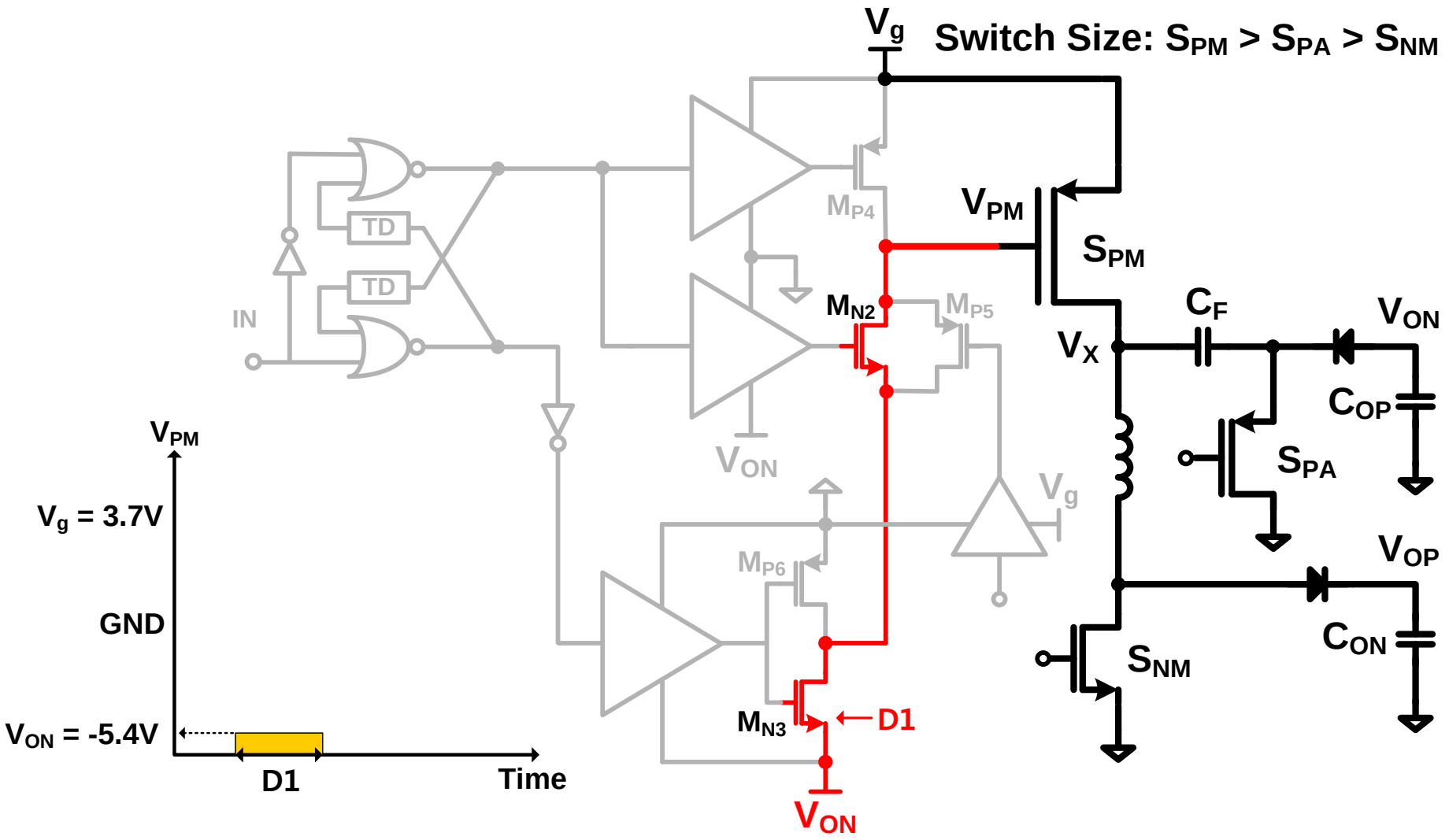
MLGD is to reduce switching loss

- To reduce the conduction loss, V_{GS} is applied as large as possible
- It inevitably increases switching loss

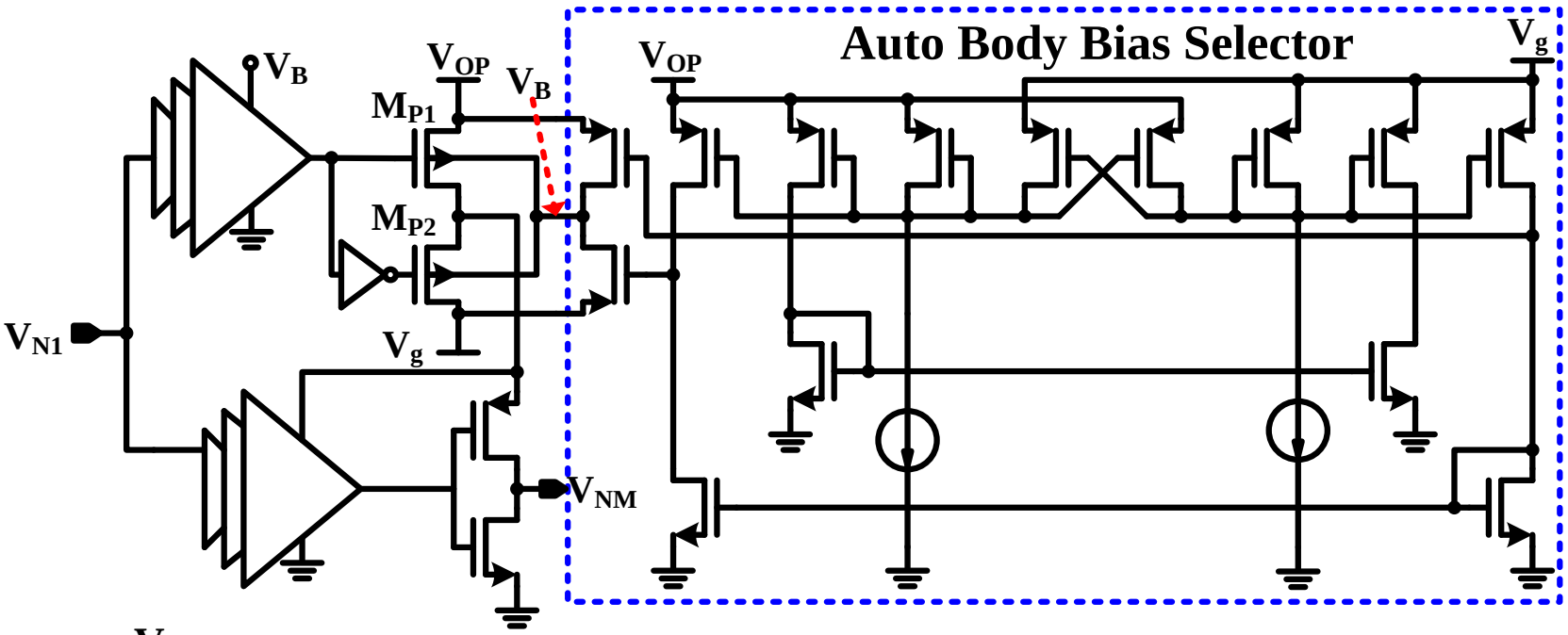
Multi Level Driving Voltages

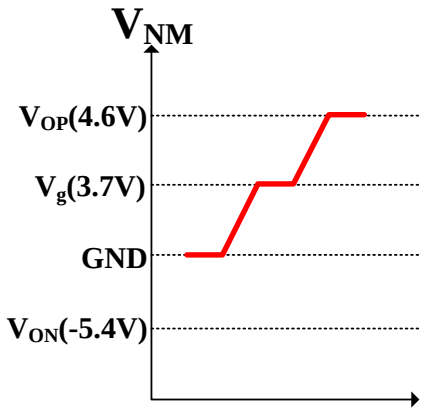


Multi Level Gate Driver for S_{PM}



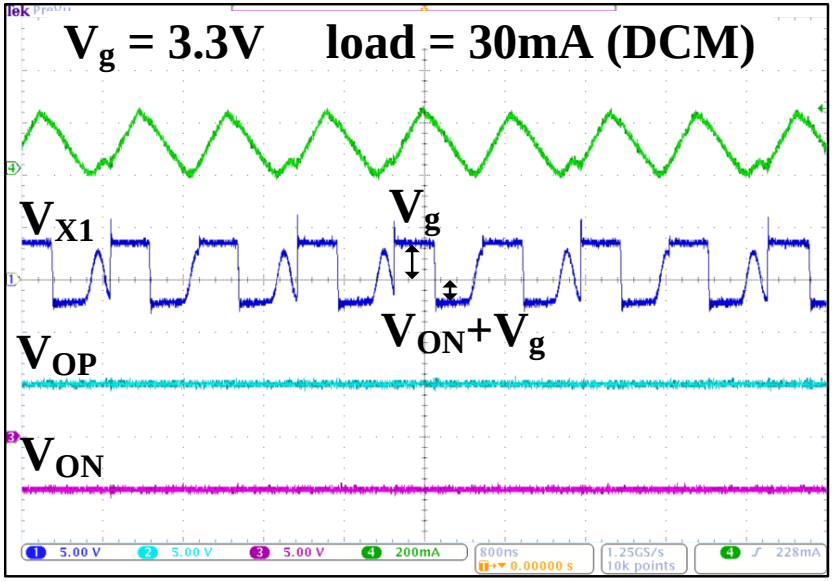
Multi Level Gate Driver for S_{NM}

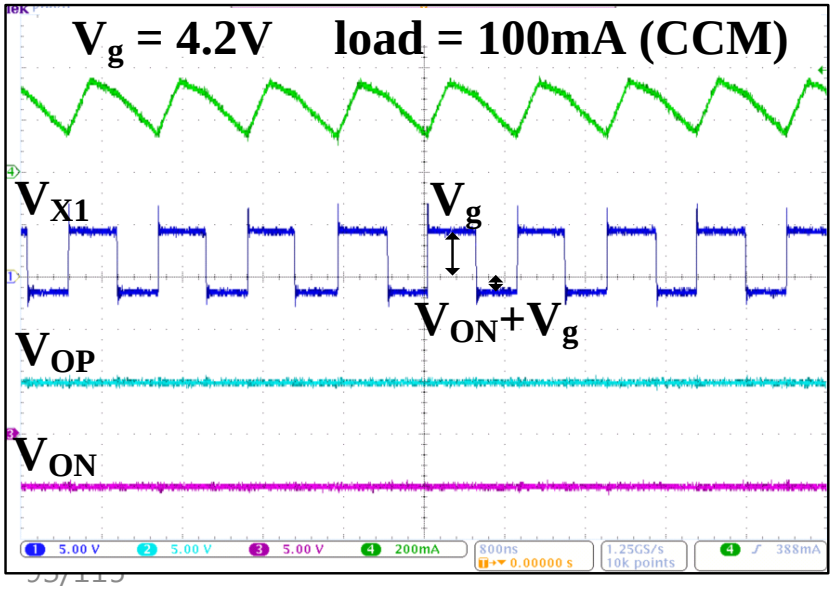


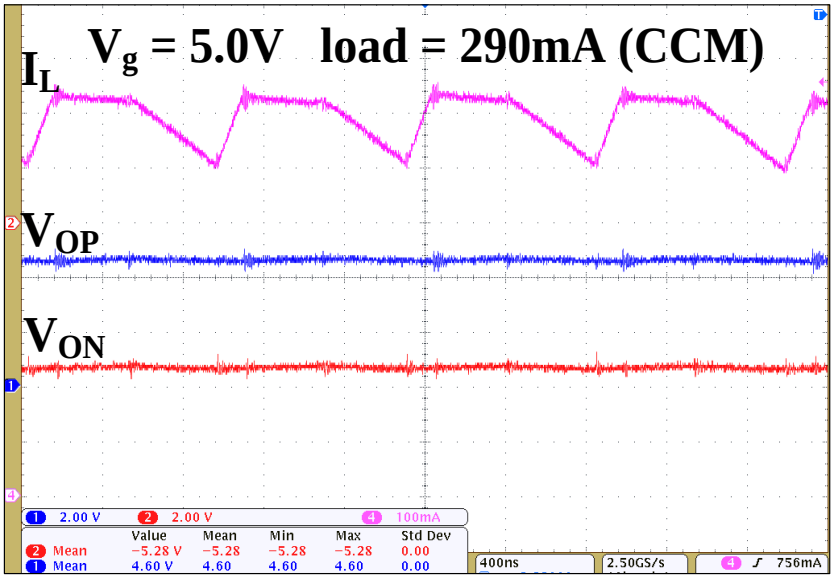


Body bias of the M_{P1} and M_{P2} is selected as the largest voltage between V_g and V_{OP}

Measurement Results







Performance Summary

Process	0.5μm BCD 1P 3M	
Supple voltage	2.7V to 4.5V & 5V(USB)	
Frequency	1.25 MHz	
Max efficiency	87.1 %@600mW	
Output	V_{OP}	V_{ON}
Voltage	4.6V	-5.4V
Max Power	3W	
Line regulation	0.3 %/V	0.14 %/V
Load regulation	0.12V/A	0.2V/A
Output ripple	50mV@300mA	60mV@300mA

Summary

- New topology about SIMO DC-DC Converter
  - Cost effective solution
  - AM-OLED Display application
  - Focus on high stability
  - Focus on high efficiency

- New control method about SIMO DC-DC Converter
  - Focus load independent stability

Thank You