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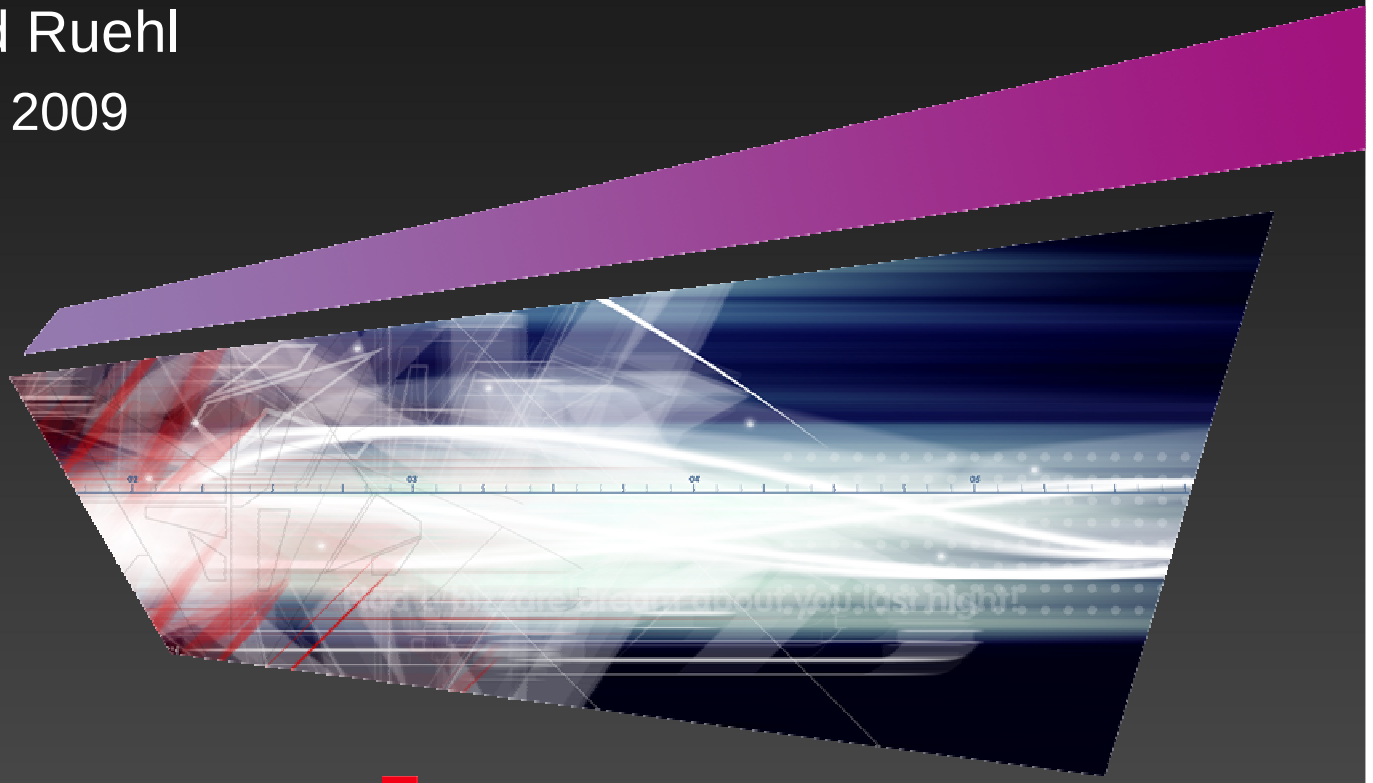
INVENTIVE

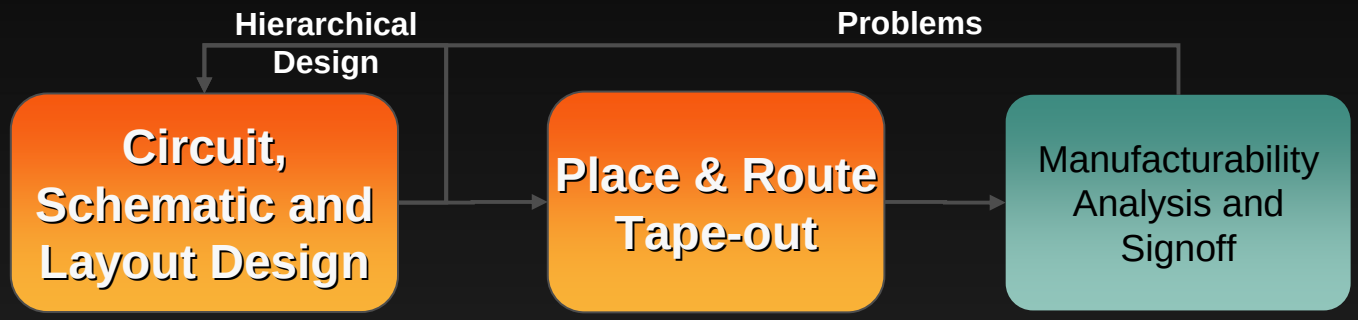
Manufacturability Analysis During Custom Design

Roland Ruehl

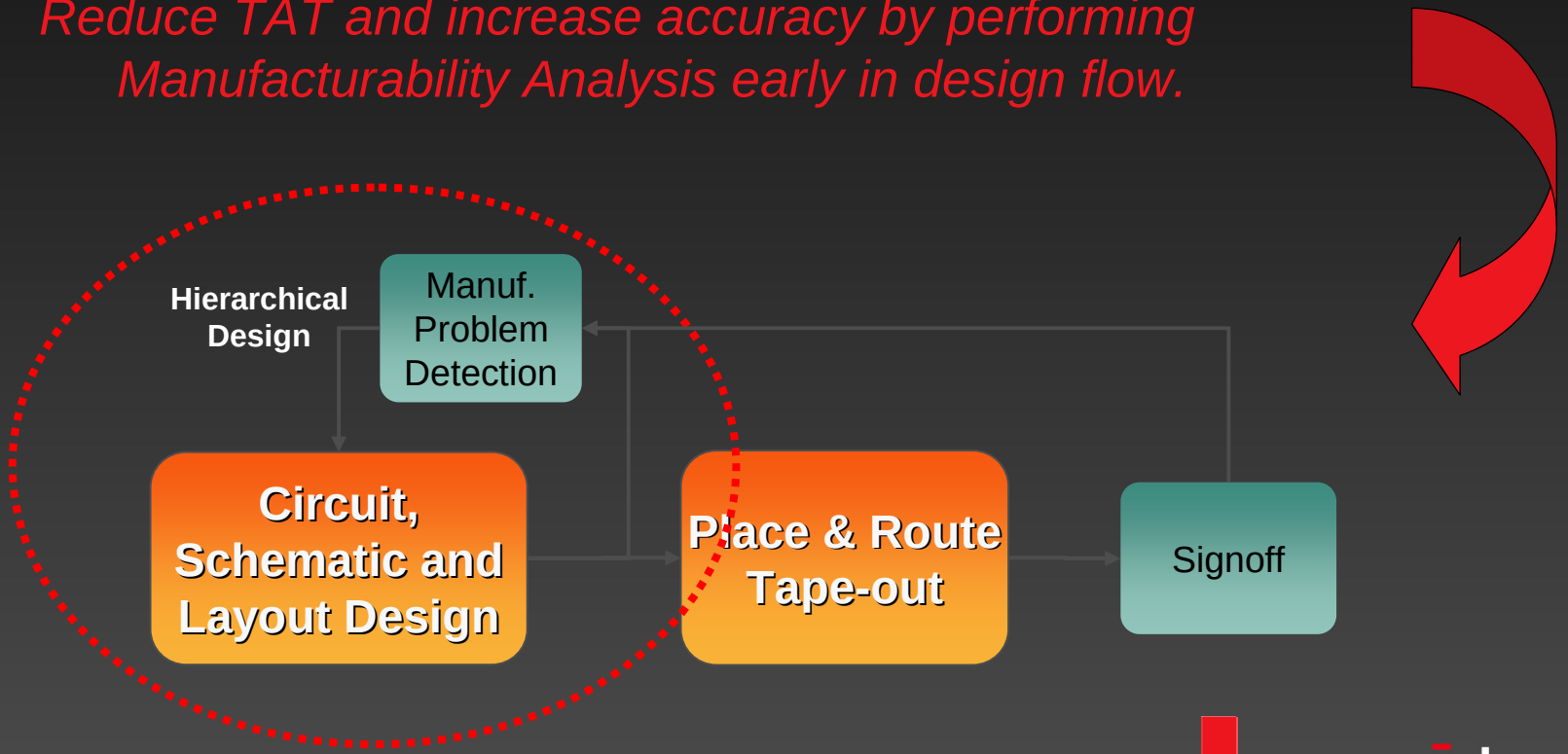
Oct 16, 2009



The Problem



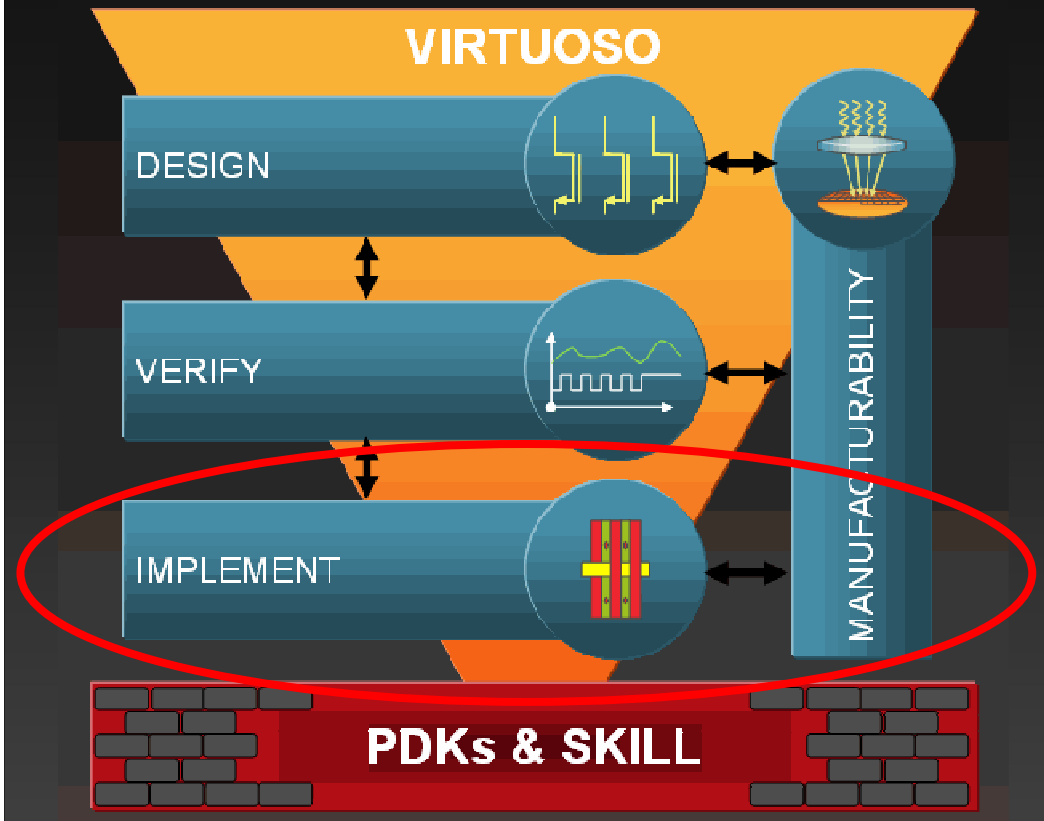
Reduce TAT and increase accuracy by performing Manufacturability Analysis early in design flow.



Outline

- The Virtuoso IC 6.1. Platform
- Manufacturability analysis
  - Effects, Impact, Models and Tools
  - Optimization
- Flows
  - Interactive Block Authoring vs. Signoff
  - Loose vs. Close Model Coupling
- Summary: Analysis and flows in IC 6.1.

Virtuoso IC 6.1 Platform
The complete and integrated custom design platform



- Launched in Oct' 2006
- All top 30 customers on 6.1
- 200+ known tape-outs
- 100+ customers in production design
- Many companies working at 40nm
- 15+ companies working at 28nm

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Manufacturing Effects and Impact

130nm

45nm

32nm

Via failure

Particle defects

Increase in catastrophic failures

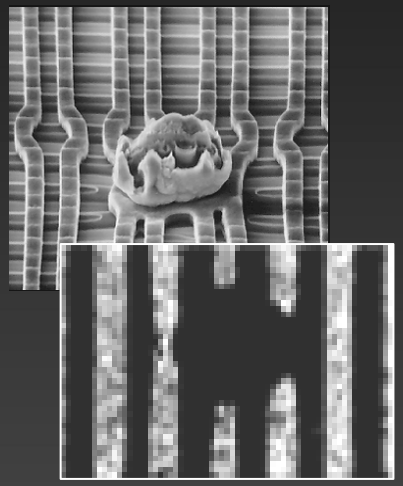
Via failure

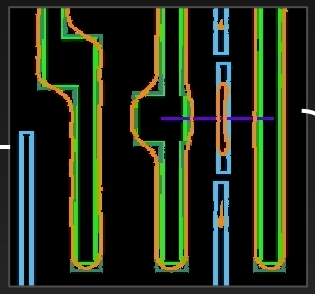
Particle defects

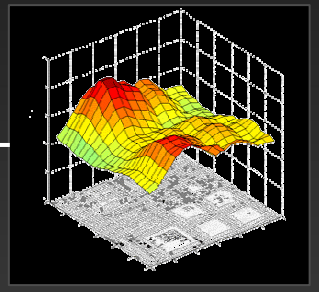
Litho and etch effects

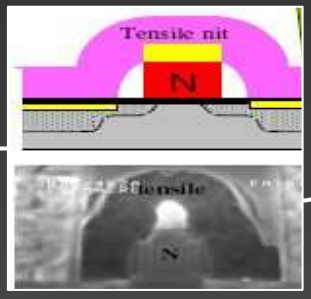
CMP effects

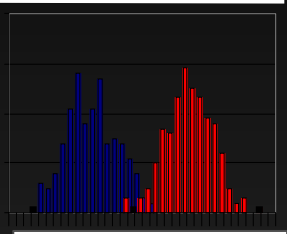
Stress effects

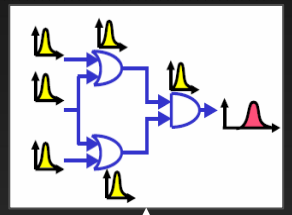










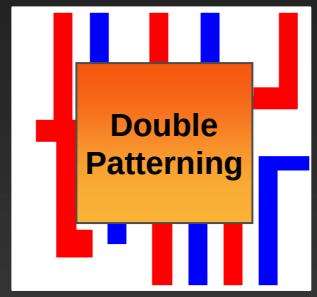


Timing, power variation

Physical changes impact electrical variation

Via failure

Particle defects



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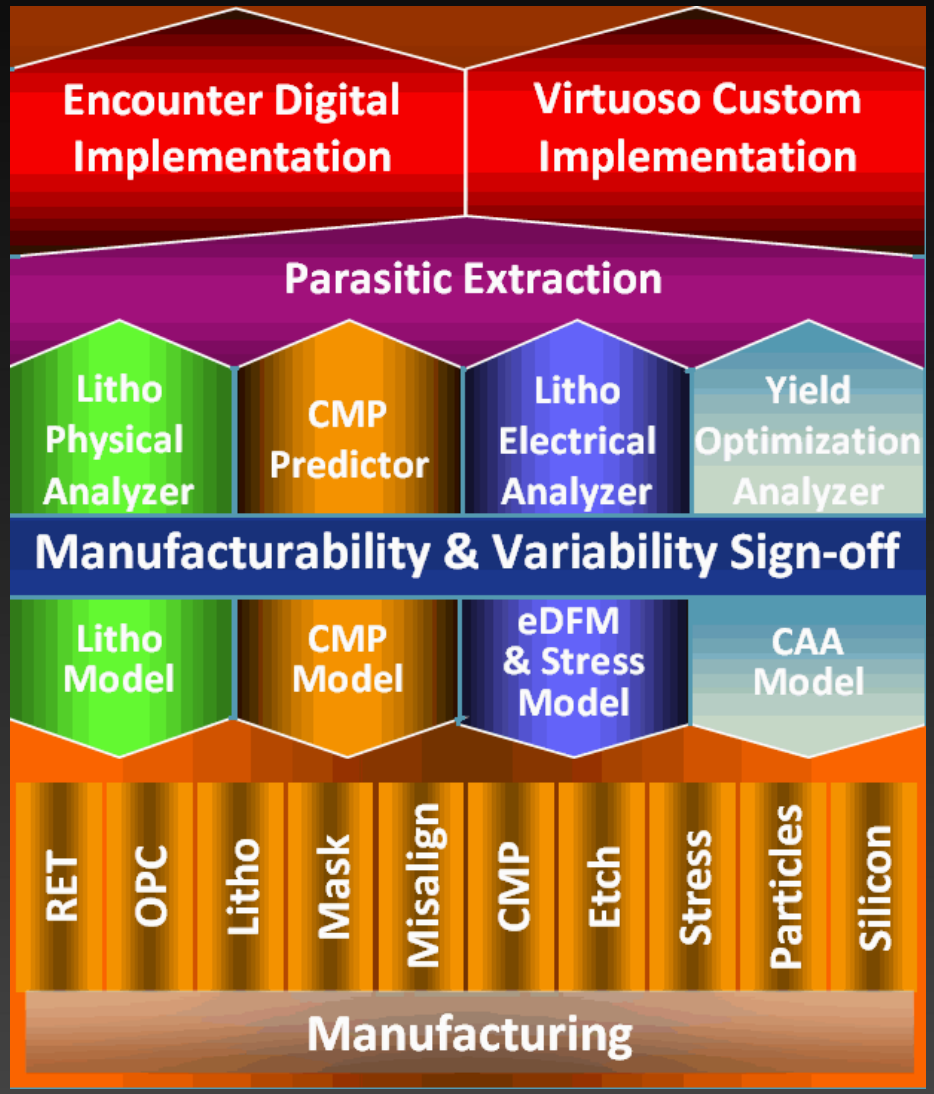
Manufacturability Modeling

- Modeling range
  - Short range (e.g. Litho) vs. long-range effects (e.g. CMP)
- Shape-based vs. Connectivity-based modeling
  - Polygon-based checking with or with-out connectivity (e.g. for Antenna checks, ESD, etc.)
- Design Rules and DRC
  - geometric modeling of most limited yield loss mechanisms
  - Mandatory rules, recommended rules, and scoring
  - To model incrementally early in design flow, design rules should be part of the design data-base (e.g. OpenAccess).
- Parasitic extraction, transistor modeling, Timing and Performance yield prediction.
- Rigorous simulation of Random Defects, Lithography, and CMP
- Present for as sign-off flows for 65nm and below and most manufacturers.

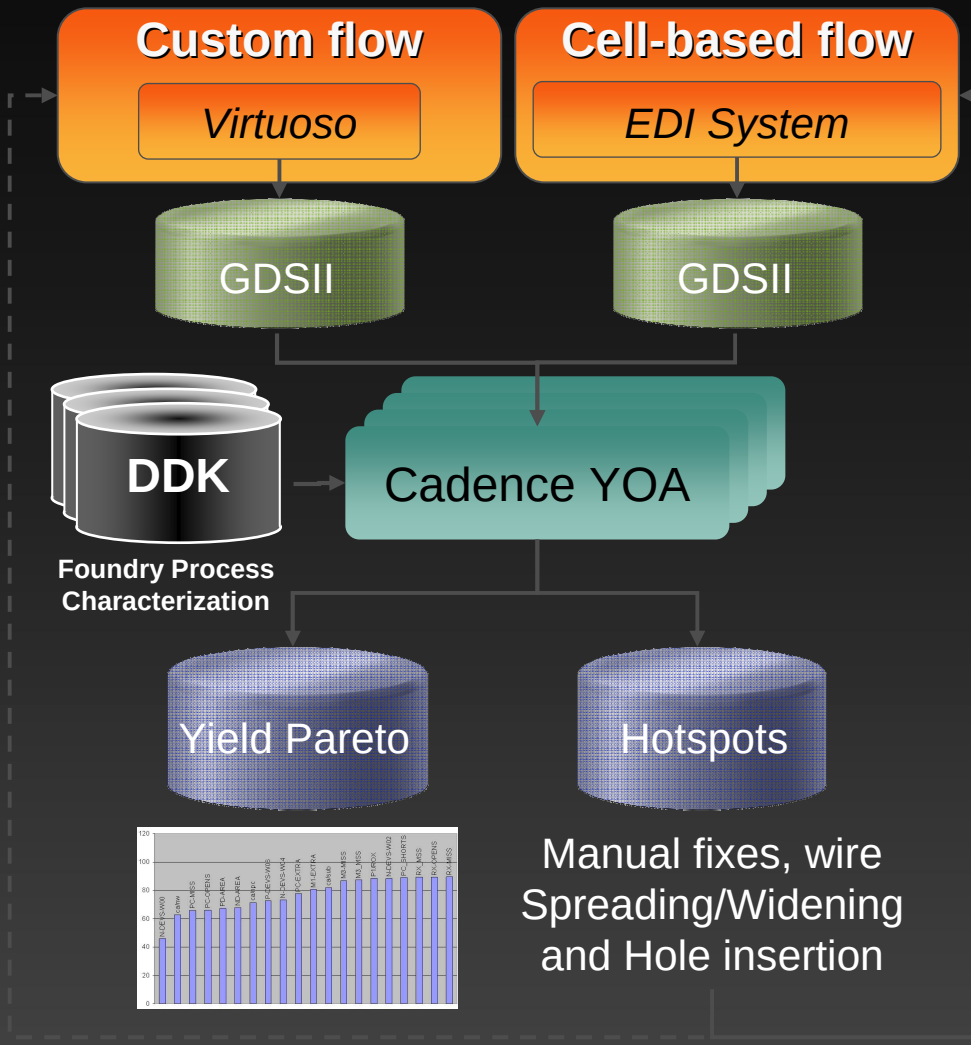
Tools

- **Cadence® Yield Optimization Analyzer (YOA)**
  - Advanced node random yield analysis
- **Cadence® Litho Physical Analyzer (LPA)**
  - **Foundry-certified** Fast and Accurate Full-Chip Hotspot Detection and Contour Prediction
- **Cadence® Litho Electrical Analyzer (LEA)**
  - **Silicon-Proven** Electrical DFM Analysis and Optimization Solution
- **Cadence® CMP Predictor (CCP)**
  - **Foundry-certified** Industry-Leading CMP Prediction Solution



Cadence® Yield Optimization Analyzer

- **Exact CAA based on Voronoi algorithm**
- **Competitive Performance**
  - used for 5 cm² 45nm production tape-outs, among others.
  - New sampling algorithm
- **High parallelism**
- **Connectivity-based CAA** opens, shorts and via analysis.
- **Flexible underlying rule language**
  - Supports variety of yield models
- **Qualified at UMC and TSMC** for 65 and 45nm production processes; at **IBM** in production down to 32nm.



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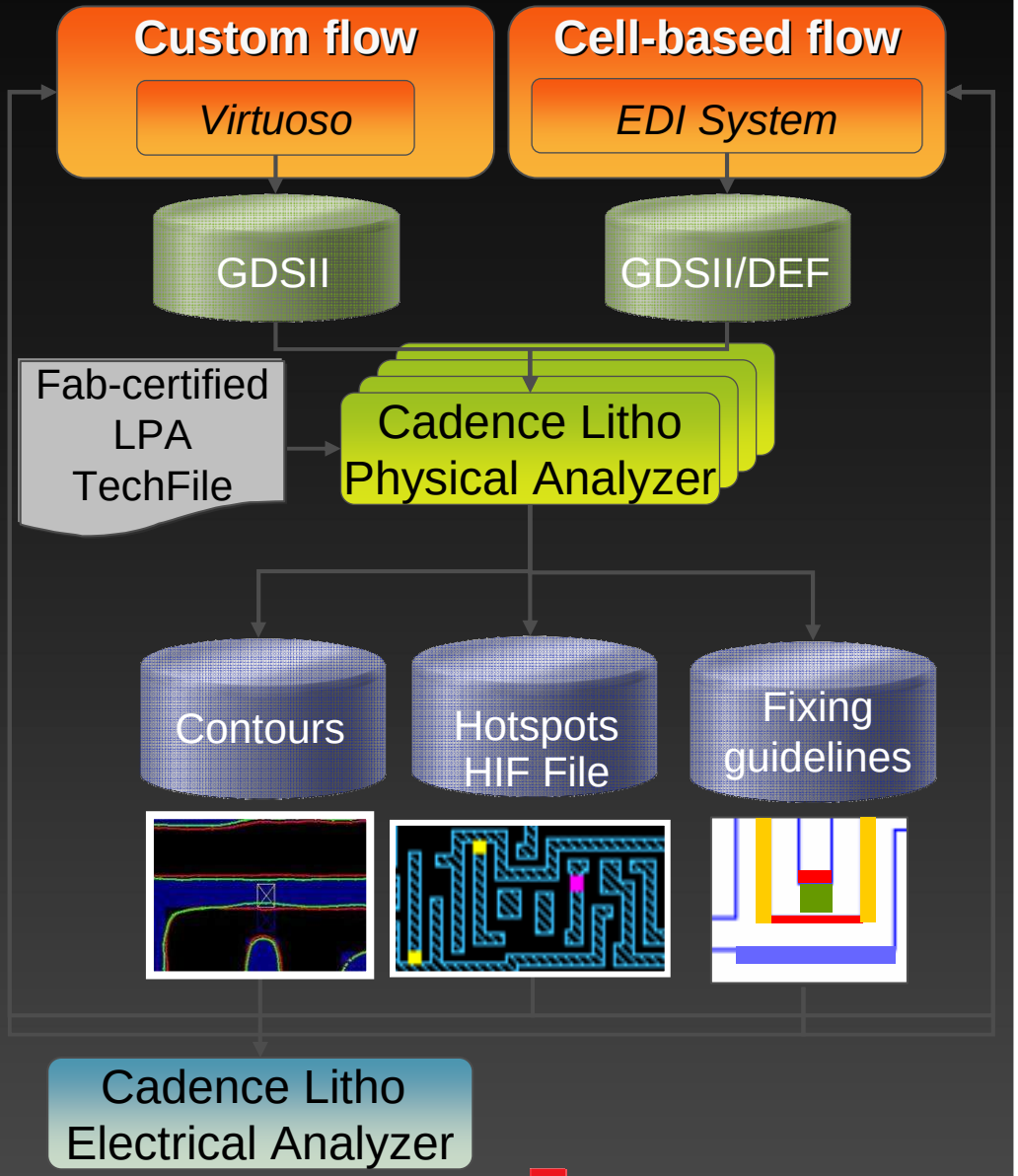
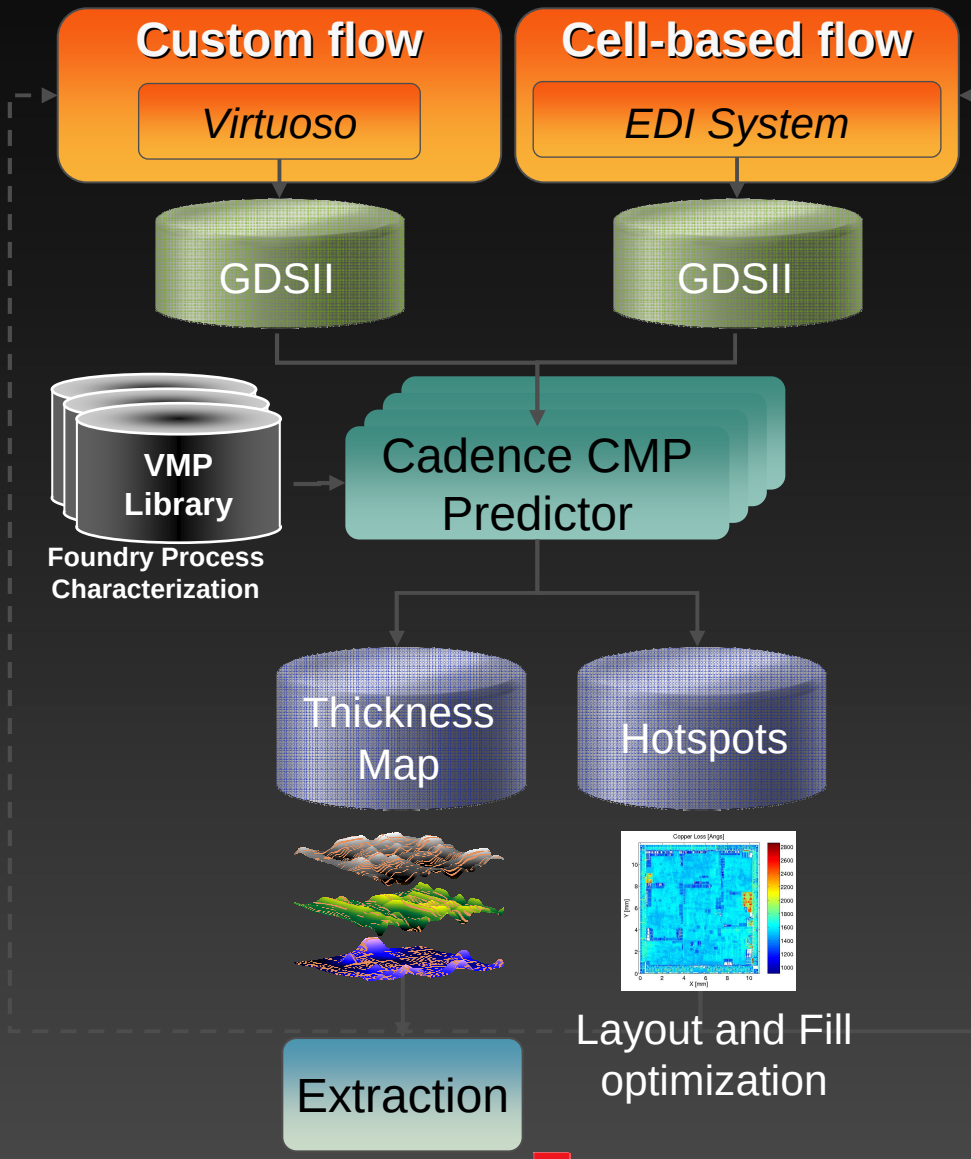
Cadence® Litho Physical Analyzer

- Leading solution for full-chip litho **sign-off**
- Detect litho hotspots and produces fixing guidelines
- Fast silicon-accurate contour shape prediction across process window
  - 4x to 30X faster
- Integrated into EDI System and Virtuoso for automatic fixing



Cadence® CMP Predictor

- Full chip interconnect and dielectric thickness prediction
  - Semi-physical based process model
  - Calibrated for specific process
  - Multi-level and long-range effects – neighboring die and scribe lines
- Manufacturing Hotspot Checking
  - Hotspot checking – Foundry defined or customer defined
  - Validated flow for design/dummy fill modifications
- RC Extraction Interfaces
  - Generic thickness export file
- Only tool qualified at all major foundries

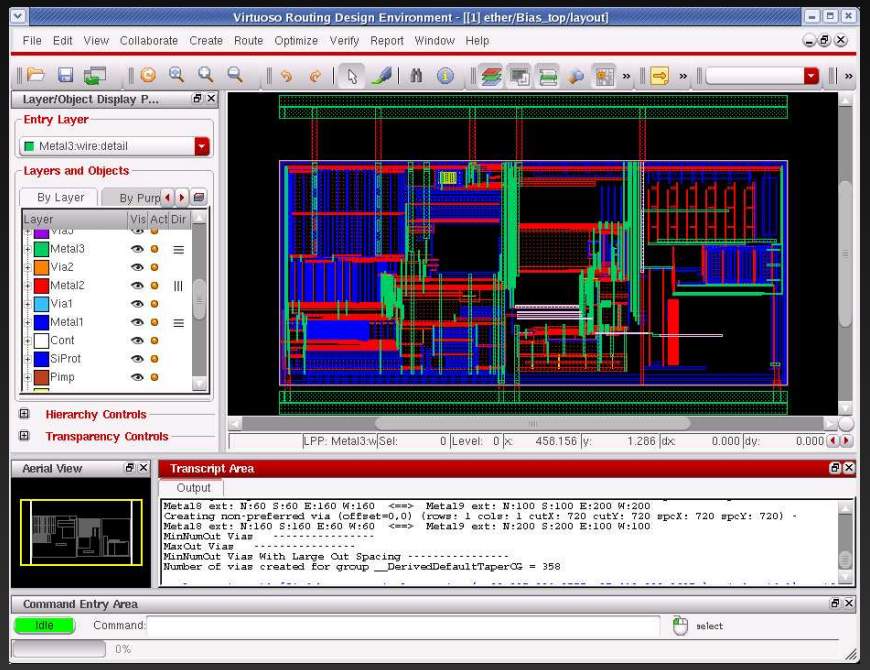


Optimization

- Changes of existing geometries
- Overlay of correcting geometries; possibly late in the design flow.
- Manual, semi-automatic and automatic optimizations
- Pattern detection and replacement; complete cell or macro replacement
- Optimization of critical nets only
- Tool-specific optimizations
  - Hole reduction and insertion; wire spreading and widening
  - Smart fill (CMP)
  - Contour-based optimizations (Litho)
- Compaction
- Re-routing (incremental or larger range)

Optimization via Routing:
IC 6.1.4 Router Development Environment

- Expert environment for developing advanced mixed-signal & structured custom routing scripts
  - TCL or SKILL based interface
  - Takes advantage of VSR VM
  - Scripts developed by experts can easily be run by general layout engineers in Virtuoso
- Advanced process rule support
  - Router and Checker
  - Investigation and development for 32/22nm
- Excellent debug environment



Router Development Environment (RDE)

Prior to 6.1.4 available via stand-alone Cadence Space-based Router (CSR)

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Custom block authoring vs. Signoff

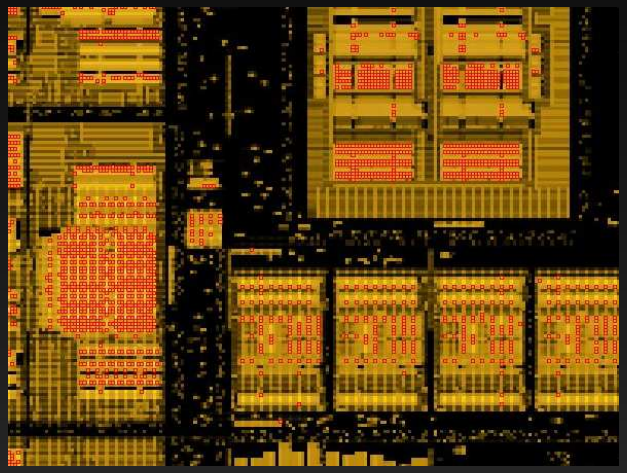
- Different performance requirements
  - Sign-off: high capacity, high bandwidth, many CPUs
  - Current GDS size around 100 Mbytes for 45nm
  - Interactive custom block authoring: smaller data size, low latency, designer's work station
- Some possible difference in modeling: schematic and connectivity information can be integrated easier early in the design flow (since part of the same design data-base).
- **Models are always evaluated and qualified in sign-off context**

Loose vs. Close Model Coupling

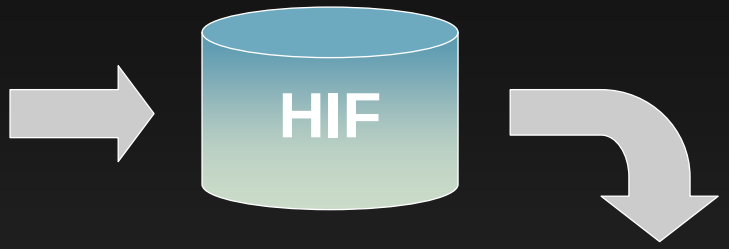
- "Loose Coupling"
  - Custom editing environment communicates with stand-alone tool, communicating via stream files (GDS/OASIS), hotspot information (HIF: location, shape and fixing hints), and other analysis output.
  - Most practical for longer-range effects or longer-range optimizations
  - Examples: CMP simulation, late Litho simulations (violations likely to happen in cell placement context), wire spreading and widening.
- "Close Coupling"
  - Custom editing environment communicates with analysis engine via design data-base (OpenAccess) or in-core API. More data can be shared with higher bandwidth and lower latency.
  - Most useful for in-situ, incremental checking and correction, and when schematic and geometric data need to be shared.
  - Examples: DRC, parasitic extraction, contour-based Litho simulation very early in design flow (cell creation)
- Early, incremental DRC can substitute for rigorous simulation of many effects (for example CMP).

Loose Coupling Example:
CYOA: From Heat-maps to Layout Fixes

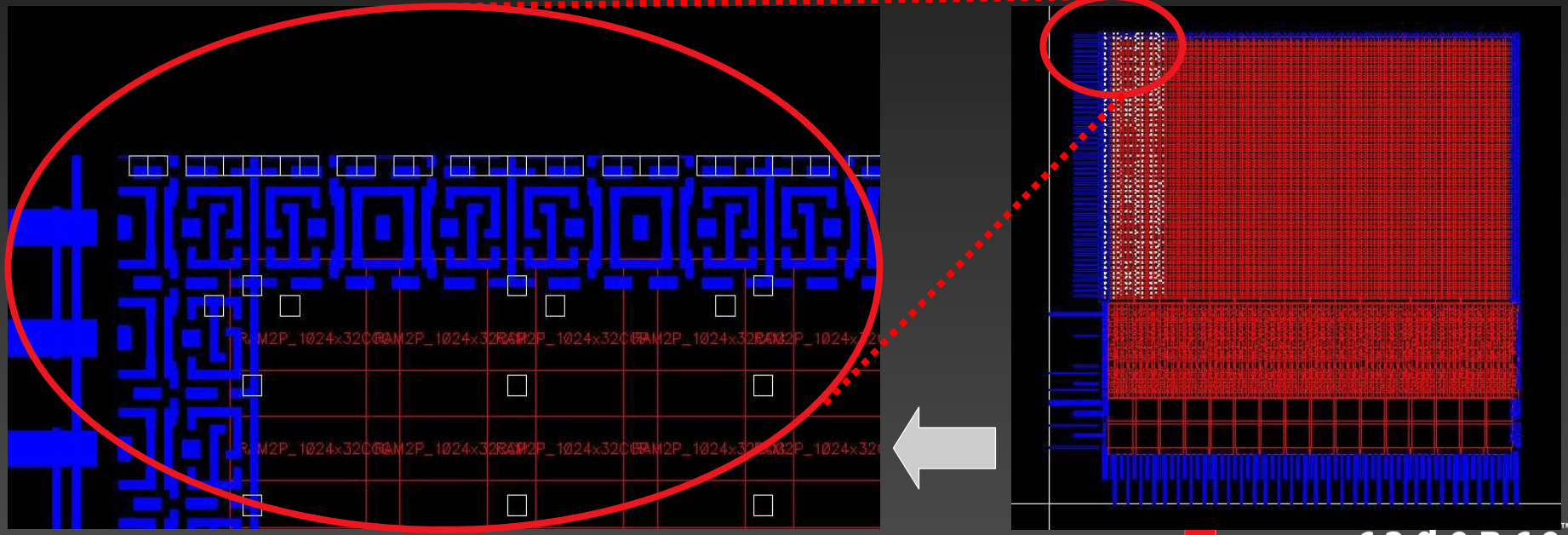
CAA Heatmap



Error Markers via Thresholding; error browser integrated within Virtuoso.



Virtuoso Marker/Shape Overlay (1st 1000 errors)



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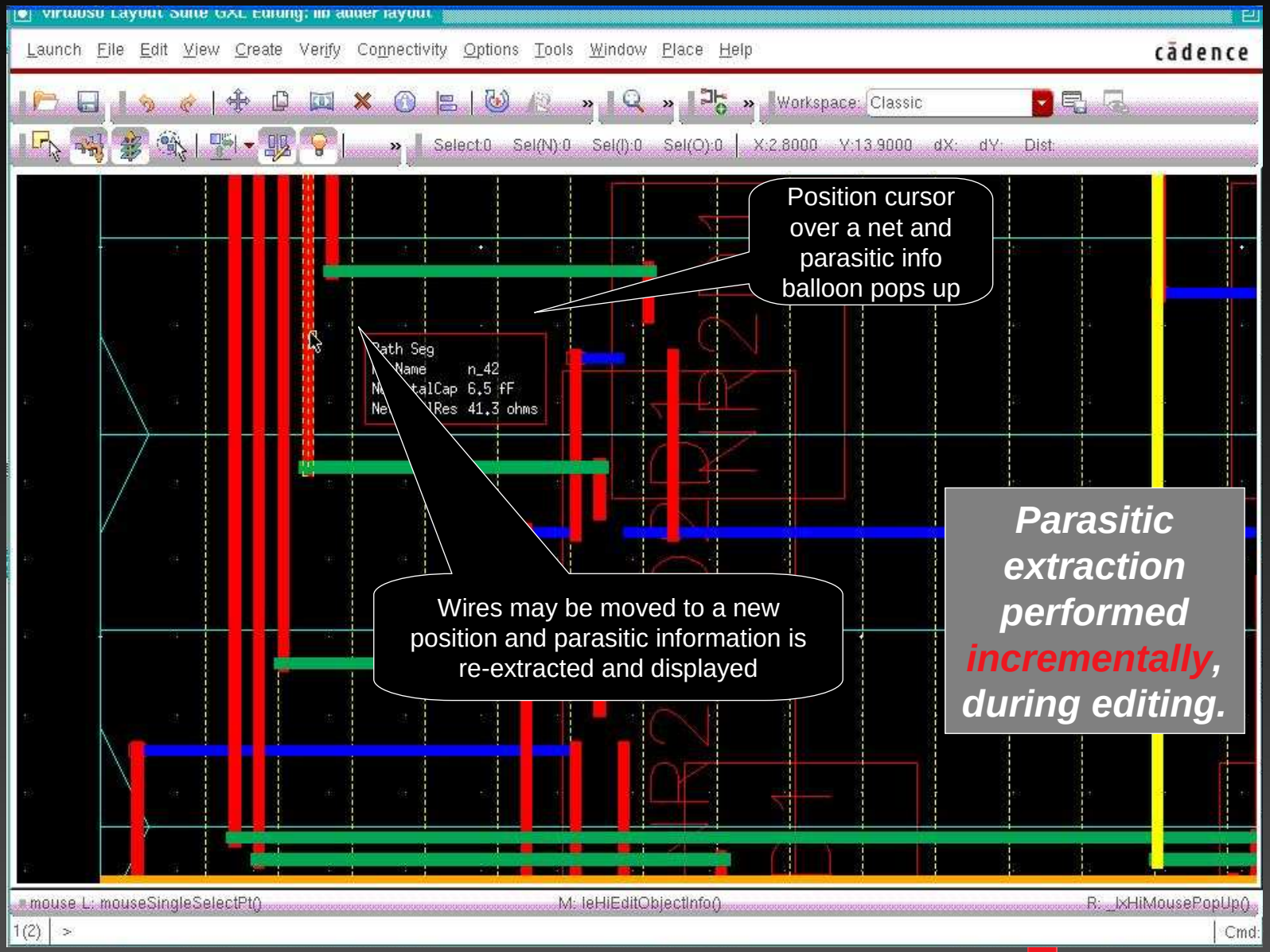
Close Coupling Example:
Incremental Extraction - Prototype working



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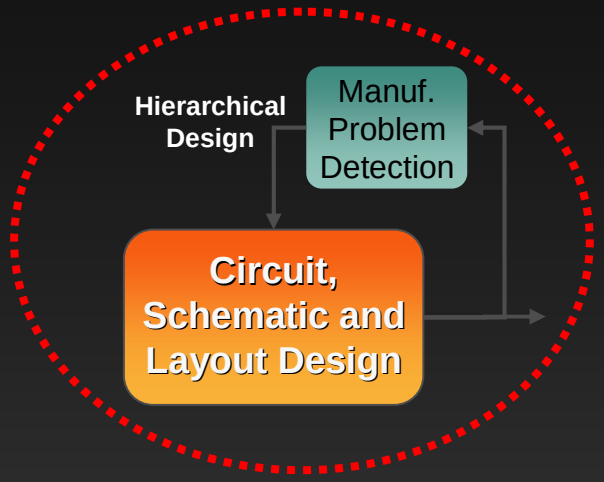
- Virtuoso IC 6.1.4: a powerful platform to perform manufacturability analysis early in hierarchical custom design.
  - Design data-base; Incremental DRC; Connectivity-aware
  - Custom block Routing Design Environment
  - Loose and effective coupling to most important sign-off quality yield simulation and optimization tools
  - DRC, Parasitic Extraction, Defect-limited Yield, Litho and CMP modeling, Pattern detection, hole optimization, spreading and widening, compaction and routing, etc.)



- On-going development
  - Incremental extraction and more accurate rule checking
  - Added custom routing and optimization capabilities
  - Close coupling of additional analysis and optimization engines